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Test & MEASUREMENT WORLD

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Henry Klim (left), executive director of the Bennington Microtechnology Center, and Dr. Harry Stephanou, director of the Automation & Robotics Research Institute and BMC founder and chairman.

TAKING MEMS SENSORS TO MARKET

The Bennington Microtechnology Center, in conjunction with its academic partner, develops the processes that bring MEMS devices from concept to commercialization.

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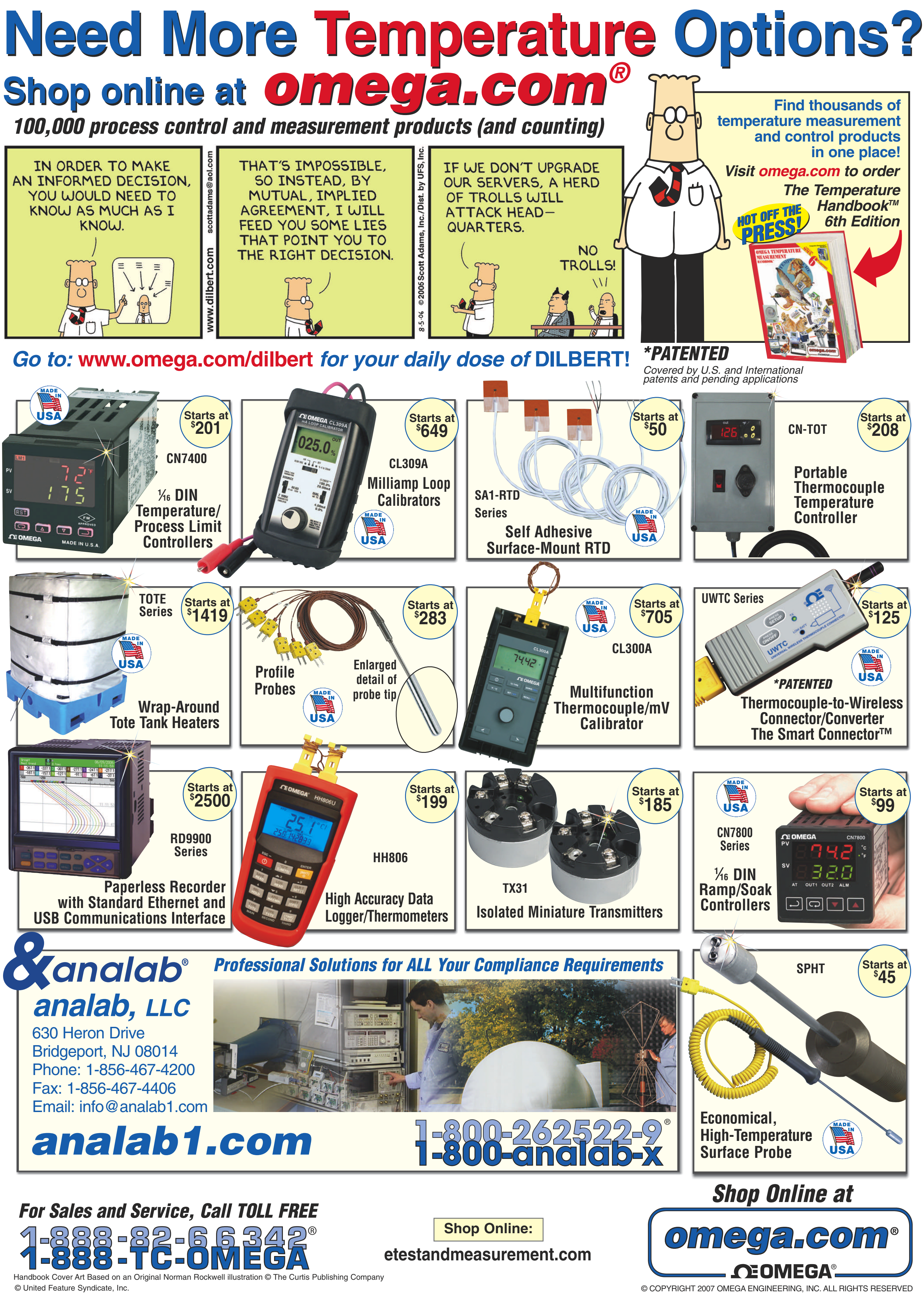

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COVER BY: AL FERREIRA

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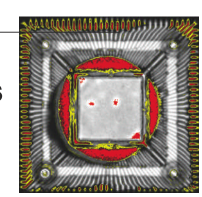

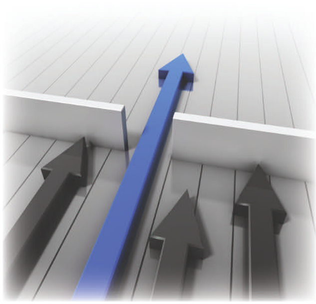

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Guest commentaries

Design automation reshapes the foundry-client dynamic

Silicon-foundry participation in design is enabling the implementation of volume diagnostics that drive improvements in manufacturing yield, reports Chris Allsup of Synopsys.

From potential energy to value added by test

Using test to screen scrap from a production line to make a final product is not fundamentally different from extracting silicon from its dioxide in order to make wafers, according to Dr. Fang Xu of Teradyne.

www.tmworld.com/guests

How does your salary compare?

SALARY SURVEY 2007

Check out the results of our 2007 Salary Survey to learn whether your salary and benefits are competitive with the rest of the test-engineering industry.

www.tmworld.com/salary2007

Blog commentaries and links

Taking the Measure

Rick Nelson, Chief Editor

- Supply and demand vanquished, Jobs tackles network effect
- Jobs repeals law of supply and demand

LXI: Instruments and Applications

moderated by Rick Nelson, Chief Editor

- Should the LXI Consortium certify software?
- LXI cuts size and complexity of video matrix

www.tmworld.com/blogs

Take a T&M Challenge

RF Challenge begins in October

Respondents who answer our monthly Oscilloscope Challenge question correctly will be entered into a drawing for an Apple iPod, courtesy of Yokogawa. Those who answer our new RF Challenge correctly will be entered into a drawing for a TomTom ONE navigation system, courtesy of Keithley Instruments. New challenge questions every month!

www.tmworld.com/challenge

Go/no-go testing is no-go

The time of pass/fail testing is history. Although it's still necessary to weed out bad parts, that's only a small component of the modern test process.

Janusz Rajski, chief scientist and director of DFT engineering at Mentor Graphics, said in a recent interview that adaptive test and advanced diagnostics are becoming critical as processes shrink. Rajski, who serves as program chair for this year's International Test Conference (October 21–26, Santa Clara, CA), said attendees at this year's ITC (www.itctestweek.org) will learn specific techniques they can apply to cope with the "staggering complexity and small feature sizes of 65-nm devices." (Read the interview at www.tmworld.com.)

RICK NELSON, CHIEF EDITOR

The goals of a modern test process are twofold (at least). One goal is to improve test coverage, and that's where adaptive test comes in. Rajski described adaptive test as an approach in which you perform analysis as well as test to determine the most frequent ways in which devices fail; based on your analysis, you try to develop more effective subsequent tests.

Test adapts to the staggering complexity of 65-nm devices.

Another goal is to improve design and production processes, which is where advanced diagnosis comes into play. Rajski said that technologies are emerging that provide links to the physical domain. Those links enable diagnosis down to the level of specific layout features to help in the calibration of DFM rules and in the development of design guidelines.

The key lesson from emerging test technologies is that test yields value. In an online column (www.tmworld.com/guests), Dr. Fang Xu, senior scientist at Teradyne's Semiconductor Test Division, makes the case that even a simple pass/fail test "is at least as important and valuable as any other stage in production," adding that screening good parts from bad "is not fundamentally different from extracting silicon from its dioxide in order to make wafers."

As engineers deal with the staggering device complexity that Rajski cited, new challenges are emerging. According to Tom Farkas, president and founder of Metrikos, the focus today is shifting to test of devices that acquire environmental or other external nondigital information, with analog stimulus in and bits out—often over an RF link. As described in this month's cover story, Farkas is working with the Bennington Microtechnology Center to develop test strategies for such devices.

However these strategies develop, you can be sure that significant benefits will come from the effective analysis and use of test results. Also in this month's cover story, BMC executive director Henry Klim emphasizes, "There is significant value in acquiring physical test data from functioning devices." T&MW

Post your comments at www.tmworld.com/blog.

(ADVERTISEMENT)

HIGH-SPEED TEST

(Loop)back to the future

New test methods tackle ≥6.4Gbps data rates

Tom Vana, Member of Technical Staff
Credence Systems Corporation
tom_vana@credence.com

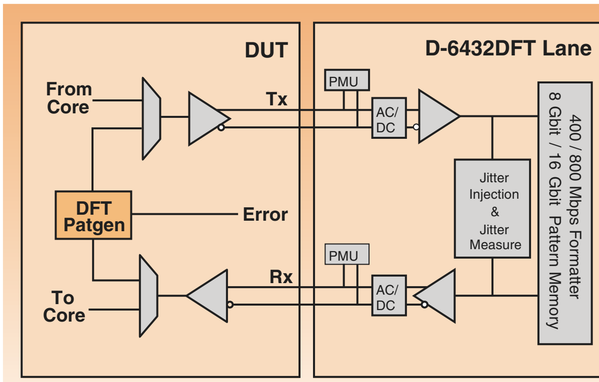
High-speed serial buses like PCI Express and HyperTransport introduce tough challenges for test engineers developing test sets with sufficient fault coverage at a cost of test the market will bear. Simple design-for-test (DFT) methodologies were implemented quickly at very low cost with limited fault coverage, while older "functional" test flows on high-end ATE platforms offered the most thorough fault coverage, but at increasingly prohibitive cost of test, test complexity and cycle times. Functional testing is becoming even less viable as cost per pin rises with bus speed in high-speed data applications, particularly in volume production test.

To meet the cost of test metrics that are established market realities, manufacturers have turned to loopback techniques (i.e., using the device to source the test data and receive it back into the device for recognition) for testing today's high-speed buses. Implementation of loopback is especially critical, considering the typical loss budget for high-speed signals. This loss budget typically has three components — contributed by the transmitter, receiver, and interconnect—all of which could degrade the signal "eye" over the loopback path and impact coverage.

Alternative DFT techniques like "near-end loopback" have already introduced cost efficiencies (via ease of programming and reduced capital investment in ATE) in testing devices for high-end consumer and computing applications. Near-end loopback techniques can be self-contained within the DUT with pathways created between the I/O pins. However, the inherent cost savings and simplicity carry stiff tradeoffs in terms of coverage. There are no parametric measurements, a lack of signal control, and lower likelihood of catching faults related to signal integrity or bit errors. For example, a simple internal or load board loopback would allow a marginal receiver to "hide" in the shadow of a robust transmitter and pass the loopback test screen. While these uncertainties can be worked around at lower speeds, compromising coverage at ≥6.4Gbps is simply too risky.

Far-end Loopback: Production-Level Testing at Lower Cost

Between the two extremes, innovative techniques such as far-end loopback combine the flexibility of DFT with the more in-depth diagnostics of functional testing. Lengthening the feedback path by placing the DUT in communication with a cost-effective, intelligent tester makes production-level testing of high-speed buses viable for the first time. Even more compelling, far end loopback with programmable signal degradation can be employed to cut costs and speed time-to-market while adding unprecedented fault coverage to loopback methodologies.

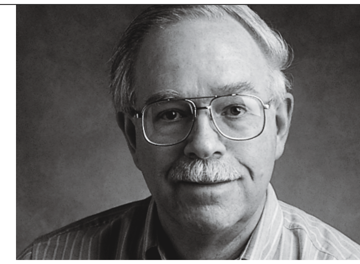


The Credence Sapphire D-6432DFT cost effectively tests high-speed buses such as PCI Express I & II, HyperTransport 1.2, 2.0 & 3.0 at data rates up to 6.4 Gbps.

Clearly, exponentially faster bus speeds are driving fundamental shifts across the board, from design through production. Innovative test methodologies like far-end loopback transform test into enabling technology and drive closer collaboration among the supply chain.

Get your FREE copy of "High-speed Bus Fundamentals" at www.credence.com/loopback

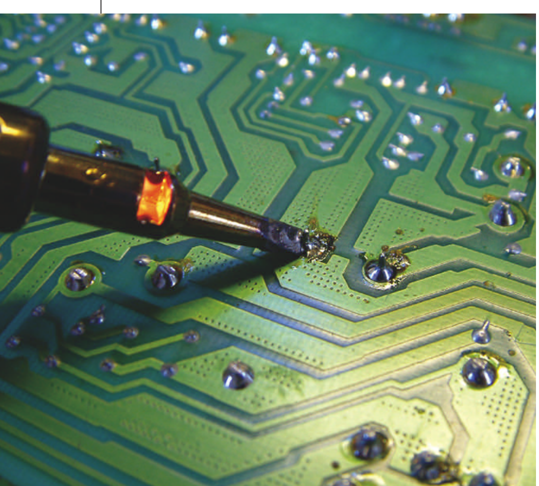
BRAD THOMPSON
CONTRIBUTING TECHNICAL EDITOR
brad@tmworld.com



Lead-free? Not so fast

Lead surrounds us. Lead and other high-atomic-weight ingredients blended into CRTs' glass funnels and faceplates help suppress soft x-radiation. Also, heirloom "crystal" glass wine goblets, vases, serving dishes, and paperweights in our homes contain lead.

In the 1920s, petroleum companies sold leaded gasoline to solve automobile-engine knock and valve-wear problems. Structural and decorative paints contained lead compounds, and lead pipes carried drinking water. Further back in time, lead sealed food cans and served as a component of pewter dishes. Romans used lead to solder water pipes.



Ahh, yes…solder. Now that RoHS and WEEE have kicked in, exotic alloys are supplanting tin-lead alloy solder in electrical and electronics applications. We've had a century of experience with tin-lead solder and thus understand its chemistry and behavior. Now, we're switching to tin-silver solder and other formulations that we don't understand as well. Tin propagates crystalline whisker growth, and silver forms interesting compounds with sulfur. The increased rigidity of tin-silver solder joints may cause fracture problems under thermal cycling.

I'm concerned that removal of lead from solder presents a reliability disaster in waiting—a wave of product failures caused by bad solder joints. I suppose that those of us in the electronics-test profession shouldn't complain, as a new technology's problems offer business opportunities and new generations of inspection instruments to play with. In the future, desktop x-ray solder-joint scanners may take their place alongside oscilloscopes as everyday test equipment.

To solve the electronics-lead problem, let's encourage consumers to recycle castoff electronics and not toss them in the trash. Hefty rebates for recycled products will work better than education alone. Otherwise, failed and castoff silver-soldered products (and their byproducts) will end up in landfills and incinerators anyway.

If we truly understood the human cost and environmental damage inflicted by the products we use and discard every day, reuse and recycling wouldn't be merely "good ideas"—they'd be sacraments. T&MW

NEVER HOLD SOLDER IN YOUR MOUTH, AND OTHER THINGS NOT TO DO WITH LEAD

Make no mistake about lead: It's a pervasive and persistent poison. But unless you were born (and currently live) in a sealed bubble, you have absorbed lead and lead compounds from your environment as you grew to adulthood:
www.nlm.nih.gov/medlineplus/ency/article/002473.htm.

This document provides links to lead-related sites, including information on recent consumer-product recalls (e.g., Chinese-made lead-painted toys):
www.idph.state.ia.us/wic/frifacts/lead_websites.pdf.

How to preserve antique tin-lead dishes (will soldered connections last as long?):
nautarch.tamu.edu/class/anth605/File14.htm.

According to popular conceptions, collective lead poisoning caused the fall of the Roman Empire. But did it?
penelope.uchicago.edu/~grout/encyclopaedia_romana/wine/leadpoisoning.html.

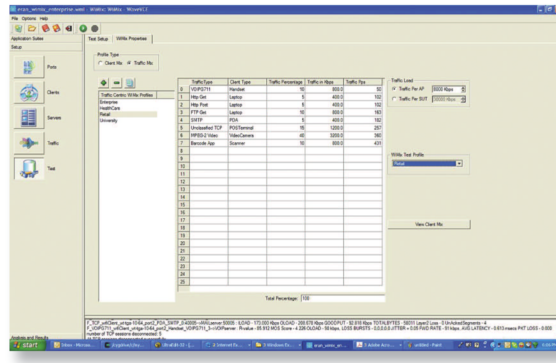
Lead poisoning helped hasten Ludwig van Beethoven's death:
www.npr.org/templates/story/story.php?storyId=5041495.

Tin grows whiskers:
nepp.nasa.gov/whisker/background/index.htm.

Tips of irons used with tin-lead solder last as much as five times longer than tips of irons used with lead-free solder. For a discussion of lead-free solder's effects on soldering-iron tips, go to:
www.elexp.com/tips/Weller_Coping_with_Lead_Free.pdf.

X-ray inspection finds solder faults:
www.tmworld.com/article/CA6470928.html.

VeriWave adds open-air testing



VeriWave reports that it has integrated its WiMix performance prediction tool for wireless Quality of Experience (QoE) with an open-air test methodology that uses VeriWave WT20 traffic generator/analyzer units in a real-world environment. The test methodology loads a wireless infrastructure network with traffic from thousands of users, enabling engineers to evaluate a realistic network environment. According to the company, Trapeze Networks is using the open-air test methodology to replicate various vertical-market environments in tests of its Smart Mobile technology.

With prepackaged traffic mixes that represent typical healthcare, education, office-building, hot-spot, government, and law-enforcement environments, VeriWave's WiMix leverages the capabilities of VeriWave's WaveTest platform to allow users to create, configure, and control variables impacting end-user experience and performance, including e-mail traffic, Web browsing, CRM applications, audio and video file transfers, video sessions, voice calls, scanners, and RFID asset management and tracking devices. The WiMix test suite allows the user to set predetermined Service Level Agreements for each traffic type. At test completion, WiMix reports the ability of the network to adhere to these Service Level Agreements for each of the traffic types. www.veriwave.com.

Aeroflex, Keithley unveil products at Autotestcon

Test products introduced during Autotestcon 2007 (September 17–20, Baltimore, MD) included an RF test platform from Aeroflex and a switch/multimeter from Keithley Instruments.

Aeroflex's new modular RF test platform handles wireless applications up to 6 GHz and supports activities ranging from research to manufacturing. The configurable system, which can integrate into cellular, wireless data, RFIC test, and military/aerospace test applications, encompasses PXI 3000 Series hardware modules, PXI Studio software, and a PXI instrument chassis.

See full Autotestcon coverage in our November issue and at www.tmworld.com.

The PXI 3000 Series modules extend frequency range coverage to include HF, VHF, and UHF—from 250 kHz to 6 GHz for signal analysis and from 1 MHz to 6 GHz for signal generation. The PXI Studio software generates and analyzes complex modulated signals, and has plug-ins that enable the software to analyze WiMAX OFDMA signals as well as provide general-purpose spectrum analysis. The new instrument chassis includes one system controller slot and seven peripheral PCI or PXI slots. www.aeroflex.com.

The new Series 3700 system-switch/multimeter and plug-in card family from Keithley Instruments can control up to 576 multiplexer channels in a six-slot, 2U form factor. The digital multimeter option provides low-noise measurements with resolutions up to 7½ digits. Together with a grow-

Agilent introduces LXI Class B trigger

Editors' CHOICE

Agilent Technologies has introduced what it calls the world's first LXI trigger box that enables precise synchronization over LAN for LXI Class C and GPIB instruments. When an LXI Class C or GPIB instrument is connected to the Agilent E5818A LXI trigger box, it gains the timing capabilities of an LXI Class B instrument. Leveraging the IEEE 1588 precision time protocol (PTP) synchronization, the trigger box enables subnanosecond time triggering and time stamping of events for the attached instruments. With reliable event-log data, users can trace and troubleshoot faults easily.

The LXI trigger box provides LXI peer-to-peer and multicast communication capabilities that improve test time, especially when heavy data exchanges occur between devices. The trigger box can be configured and upgraded through a Web browser.

The SCPI-compatible E5818A LXI trigger box is a stand-alone LXI Class B device and includes a bundled IVI driver. It can achieve a synchronization accuracy of up to 13 ns (standard deviation over direct connection) and provide time stamping of up to 5000 events. Each trigger box provides BNC connectivity to two instruments (any combination of GPIB or LXI Class C).

Price: $1500. *Agilent Technologies, www.agilent.com.*

ing family of plug-in switch and control cards, the Series 3700 can serve in a functional test system or in standalone data-acquisition and measurement applications. It can perform multichannel I-V testing and accelerated stress tests. www.keithley.com.

PCB Piezotronics forms automotive division

Sensor manufacturer PCB Piezotronics has formed a new Automotive Products Division devoted to the automotive test market. Capabilities covered include vehicle NVH and dynamics, vehicle and component durability, and powertrain testing applications. The new division is located in Novi, MI.

Appointed to lead the division as director of sales and marketing is Jeff Case, who was formerly chief program engineer at Ricardo North America. A formal introduction of the division will take place at the Automotive Testing Expo North America, October 21–26, in Novi. PCB will showcase an automotive technologies pavilion, with a series of demonstrations and an IndyCar display with Andretti Green Racing. www.pcb.com.

CALENDAR

Aerospace Testing Expo North America, November 6–8, Anaheim, CA. Sponsored by Reed Exhibitions. www.aerospacetesting-expo.com/northamerica.

Productronica, November 13–16, Munich, Germany. Produced by Messe München. www.globalelectronics.net/id/21310.

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

Editors' CHOICE

Logic analyzer goes PCI Express

PCI Express 2.0, the popular computer interconnect bus, uses a three-layered protocol at speeds up to 5 Gbps. To let you capture bus transactions at those speeds, Tektronix has added two PCI Express (PCIe) 2.0 logic-analysis modules to its TLA7000 line of bench and portable logic analyzers (portable shown). The TLA7S16 and TLA7S08 let you capture and analyze PCIe bus physical-layer signals and decode those signals up to protocol layer 3. The modules also let you verify that the PCIe 2.0 power management functions properly.

A PCIe 2.0 link uses one, four, eight, or 16 "lanes" that operate only as needed, thus minimizing power consumption. The TLA7S series modules capture the handshaking on the bus that manages the lanes. You can trigger an acquisition regardless of lane activation, and you can filter data to show only those patterns of interest. Furthermore, you can use the modules in conjunction with a Tektronix oscilloscope to view the analog and digital characteristics of a signal.

Data lanes consist of two paths, one for each direction, and the eight-channel TLA7S08 can capture data in both directions for links with one or four lanes. The TLA7S16 can capture data in both directions for one, four, or eight-lane links. For 16-lane links, you need two TLA7S16 modules. Tektronix has also introduced the P6708 (eight channel) and P6716 (16 channel) mid-bus probes that let you capture data at bus locations between devices.

Base prices: TLA7Sxx modules—$55,000; P67xx logic probes—$16,000. *Tektronix, www.tektronix.com.*

MARTIN ROWE
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The serial port: Alive and well

The good old serial port is alive and well, even if today's computers lack the familiar DB-9 connector. Engineers continue to use serial ports to communicate with instruments, ovens, programmable controllers, development boards, and ICs.

Engineers often prefer the serial port when connecting just one instrument to a PC. "At least 50% of my stand-alone instruments still use RS-232," said Sergey Liberman, consultant at Solidus Integration. "People still use serial ports on Windows 95/98/2000 platforms because they work," added Chris Harden of Easy-Daq when I asked an online forum of test engineers.

Serial ports may have vanished from PCs in favor of USB and Ethernet, but they haven't vanished from PXI embedded controllers. The **figure** compares a 1997 PXI controller from National Instruments to its 2007 successor. Over 10 years, one serial port has been replaced by three additional USB ports, but one serial port remains. "Our customers keep asking for a serial port," said Luke Schreier, precision DC and digital test manager at National Instruments.

Other embedded controllers also provide serial ports. Tim Rhoads, electrical engineer at BAE Systems Battery Technology Center, recently deployed a data-acquisition system that needed seven serial ports (four RS-485 and three RS-232), two USB ports, and an Ethernet port. "I was gladly surprised to find a rugged single-board computer with eight serial ports," he said.

Many microcontrollers provide serial ports because they're inexpensive to implement. "I use the serial port all the time to send and receive information from my development board," said Oscar Rivera at Intel.

Measurement instruments and other equipment that now have USB ports may still use serial ports internally. "Many newer instruments use USB-to-RS-232 chips and therefore are still programmed using RS-232," added Liberman of Solidus Integration. Converter ICs provide a virtual serial port carried over USB so that systems can use a PC's USB port without requiring a complete redesign to fully implement USB.

Other engineers report that they use Ethernet in conjunction with serial ports to reduce the number of cables in a system. For example, Alvin Moore, measurement systems programmer at Corning Cable Systems, connected several temperature chambers, which have serial ports only, to a PC through an Ethernet hub. He used an Ethernet-to-serial converter for each serial port but needed only one cable to connect them to his computer. Moore used VISA to communicate from his application program to the chambers.

"Serial ports are painful to use but easy for the instrument developer to implement," said Scott Hannahs, researcher at Florida State University.

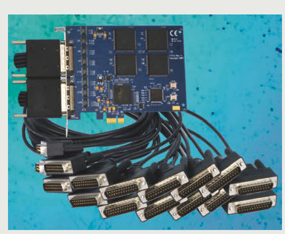
Wiring two devices with serial ports may require you to swap the transmit and receive wires (pins 2 and 3). If you have the right cable, then the serial port is easy to use, especially if you're frequently changing instruments or need to connect just one instrument to a PC. T&MW

For more comments on the serial port, see my "Rowe's and columns" blog at www.tmworld.com/blogs.

A 1997 PXI embedded controller (left) has two serial ports. The 2007 version adds three USB ports but still retains one serial port.

Courtesy of National Instruments.

PCI Express card adds 16 serial ports



Sealevel Systems has introduced the COMM+16.PCIe card, which adds 16 serial ports to desktop PCs and uses one PCI Express (PCIe) slot. The card uses one PCIe data lane but is compatible with slots that have multiple lanes. Price: $679. www.sealevel.com.

Cabled PCI Express interface cards

The OSS-PCIe-HIB2 line of cards from One Stop Systems brings PCI Express lanes out of the computer, making them available to devices and chassis that require high-speed digital ports. The cards add x1, x4, or x8 PCIe lanes. Prices start at $250. In addition, a cabled PCIe interface card for laptop computers adds x1 ($395) or x4 ($450) lanes. www.onestopsystems.com.

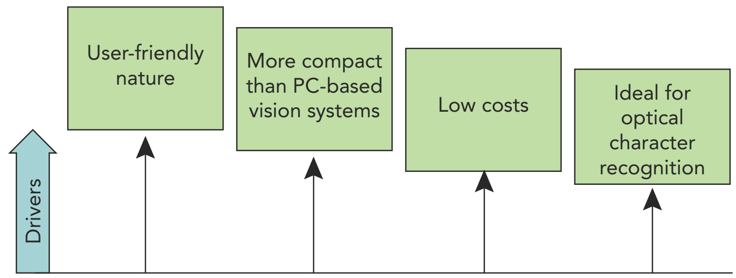
Power supplies add LXI ports

Kepco's KLP line of 1200-W, 1U rack-mounted power supplies are now available with an LXI class C Ethernet port. When ordering, simply add the extension "1.2K" to the part number. www.kepcopower.com.

JUAN ROSALES
RESEARCH ANALYST, FROST & SULLIVAN
www.frost.com

Smart cameras benefit from technological advances

SMART CAMERAS, WHICH feature built-in processors that yield high-quality images without relying on external frame grabbers, have been widely used since their inception in the 1980s. Although smart cameras are extremely valuable for flaw detection within inspection processes, the current trend suggests that they will experience an increased role in other applications, such as bar-code reading, surveillance, and noncontact measurement. This is due to the inherent benefits that make such technology desirable to end users, some of which are illustrated in the **figure**.



Smart cameras will become more attractive as technological advancements in electronics increase their capabilities and as their prices continue to decrease.

The user-friendly nature of smart cameras is perhaps the largest contributor to their success. Whereas users of PC-based systems often must maintain numerous components, users of smart cameras often have the luxury of keeping track of only one component—the camera itself. No formal computer skills are required for using such systems, and the software that accompanies smart-camera technology is easy to understand. As a result, smart cameras that feature convenient user interfaces are often preferred over more-sophisticated PC-based options.

While smart cameras will not completely displace the use of PCs in inspection processes, their compact size is satisfying a need in applications that logistically may not be conducive to larger systems. Although smaller in size, smart cameras will soon be able to achieve processing power close to that of the larger PC-based systems, due to the advancements occurring in the electronics industry.

The affordability associated with smart cameras allows end users to satisfy their inspection requirements at a reduced price. Smart cameras come equipped with a camera, lenses, cabling, processing, and, in some cases, illumination. They are generally more affordable to purchase and set up than PC-based systems, which often require a more complex network of modules. Although the addition of various elements into a smart-camera-based system may increase the overall costs, such systems are still considerably less expensive than their PC-based counterparts.

While some applications may require the fast processing speeds of PC-based frame grabbers and processors, smart cameras are suitable for optical character recognition and bar-code reading. Optimal production speeds for such activities can be achieved with current smart-camera technology. And when combined with off-the-shelf lighting sources, smart cameras are able to inspect high-volume units.

Despite the increased utility of smart cameras, there is still a demand for PC-based machine-vision inspection in complex and sophisticated applications. Looking to the future, however, the performance competencies of smart cameras will continue to increase as their processing capabilities improve, and smart cameras will be used in applications that currently employ PC-based technology. T&MW

PCB book-to-bill

The book-to-bill ratio for the North American rigid printed-circuit board (PCB) industry increased to 1.02 in July from 1.01 in June, as did the combined ratio for rigid and flexible circuits. For flexible circuits alone, the ratio dipped to 1.04 in July from 1.12 in June. www.ipc.org.

WiFi mesh networking equipment market

The WiFi mesh networking equipment market had over 100% shipment growth in 2006 and will have over 90% growth in 2007, reports In-Stat. Strong growth will continue for WiFi mesh access points (APs) for the next several years, as shipments grow more than threefold between 2006 and 2011, the market research firm says. The $3495 report titled "2007 Worldwide WiFi Mesh Equipment Market" notes that WiMAX and cellular will both negatively impact the market as these services go after the same nomadic users that public WiFi networks target. www.in-stat.com.

Semiconductor equipment book-to-bill

North American-based manufacturers of semiconductor equipment posted $1.44 billion in orders in July 2007 (three-month average basis) and a book-to-bill ratio of 0.84. The ratio stood at 0.91 in June. Stanley T. Myers, president and CEO of SEMI, said, "Orders have slowed from the strong levels observed in the first part of this year and are at levels last seen in November of 2006." www.semi.org.

WEBCAST

Meeting PCIe 2.0 physical- and protocol-layer test challenges

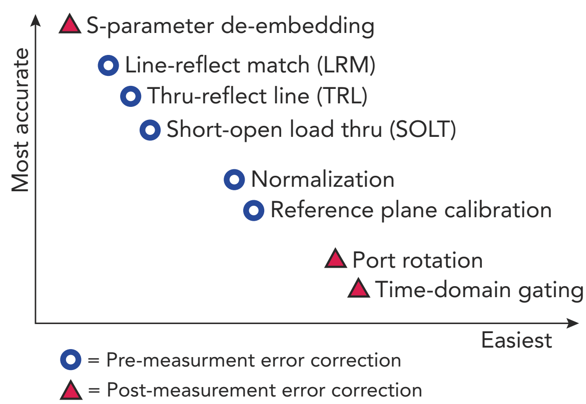
PCI Express 2.0 will enable 5-Gtransfers/s (GT/s) data rates, but as you contend with testing version 2.0 devices, you will have to deal with factors like different de-emphasis levels as well as changes to the PCIe Card Electromechanical (CEM) specification. That's the message from Rick Eads, serial applications program manager for high-performance oscilloscopes at Agilent Technologies, as he kicks off the Webcast, "Successfully negotiating the PCI Express super highway towards full compliance."

Topics that Eads focuses on include de-embedding your test fixture, which, he reports, you must do when making measurements at 5 GT/s. De-embedding, he says, is the process of deconvolving the effects of your compliance test board to yield an effective measurement at a DUT's transmit pins. He cites the advantages and disadvantages of various methods, ranging from S-parameter de-embedding to time-domain gating (**figure**).

Gordon Getty, an application engineer at Agilent's logic and protocol test group, concludes the 1-hr Webcast with a description of protocol test requirements, covering topics such as Config Space testing using the PCIECV tool provided by the PCI Special Interest Group (PCISIG, www.pci-sig.com). He covers link layer tests (a cross section of tests that, if the device passes them, would indicate a reasonable chance of interoperability) and transaction layer testing (which includes checking advanced error reporting capabilities). He also covers LTSSM (Link Training and Status State Machine) and ASPM (Active State Power Management); the latter is used to reduce power consumption in PCIe devices.

The Webcast, sponsored by Agilent, *EDN*, and *Test & Measurement World* and presented live August 29, 2007, may be viewed at www.tmworld.com/webcasts.

Rick Nelson, Chief Editor

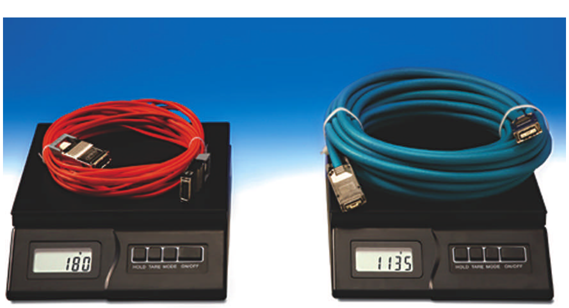


Various methods of fixture de-embedding involve tradeoffs between accuracy and ease of implementation.

FIBER OPTICS

Tests validate 100-m InfiniBand cables

Computing clusters need the highest possible data-transmission speeds between them in order to keep up with the speed of their processors. But computers in clusters, even those that use the InfiniBand I/O standard to communicate, have been limited by the transmission rates in copper cables, which are also heavy and block air flow in computer rooms.



A 100-m fiber-optic cable weighs only 180 g, considerably less than its copper counterpart (1135 g). Courtesy of Intel.

To reduce the bottleneck, engineers at Intel developed fiber-optic cables that are direct replacements for copper cables because they include optical-to-electrical and electrical-to-optical converters in their connectors. The figure shows the difference in size and weight between the red optical cable (180 g) and the copper cable (1135 g).

A demonstration of the cables took place at the International Supercomputing Conference on June 27 in Dresden, Germany. The cluster demonstration included computers from 18 companies such as Dell, Hewlett-Packard, and IBM.

Intel engineers tested the fiber-optic cables to lengths of 100 m—a 10X increase over copper cables—at data rates up to 20 Gbps using InfiniBand technology. Each connection uses four 5-Gbps data lanes in each direction. Each lane moves in a separate optical cable. The cable designers wanted to achieve a 10^{-15} bit-error rate (BER) with the

Tests validate 100-m InfiniBand cables *(continued)*

optical cable. The best BER of the copper cable is 10^{-12}.

To prove the capability of the cables, engineers performed BER tests. An arbitrary waveform generator generated transmission streams and added impairments. "With copper cables running at 5 Gbps, the eye diagram was closed after 5 m," said Tom Willis, general manager of Intel Connects Cables, in a telephone interview with *T&MW*. "With the optical cable, we observed almost the same eye opening at 100 m as at 1 m."

During a test, which lasted 5 min, a sampling oscilloscope measured jitter and calculated BER. Using a "bathtub" curve, engineers could verify that the BER met the specification. Engineers calculated that at 10^{-15} BER, a 100-m cable would produce 1728 errors per day. At 10^{-12} BER, copper cables would produce 1,728,000 errors per day.

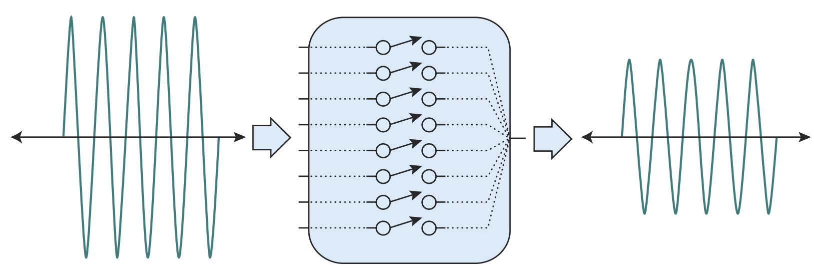
Martin Rowe, Senior Technical Editor

INSTRUMENTS

Get to know RF switch specifications

RF switches—like all other components of a transmission system—degrade signals. Signal degradation can become significant at frequencies above 1 GHz. At 3 GHz, the signal loss intensifies further.

You may assume that an RF switch's bandwidth is the 3-dB point, the point where output signal power drops to 50% of that level at lower frequencies.



RF switches attenuate the amplitudes of high-frequency signals.

Not so when it comes to RF switches, argues Jaideep Jhangiani, product manager for switches at National Instruments. In a paper titled "Understanding RF Switch Specifications," Jhangiani explains that "bandwidth is the highest-frequency signal that the manufacturer believes you can route through the product with acceptable performance."

In the paper, which you can download from the online version of this article (www.tmworld.com/2007_10), Jhangiani explains that bandwidth isn't the only specification you should investigate in an RF switch. He describes how the characteristics of a transmission line affect signal integrity. Specifications include impedance, insertion loss, voltage-standing wave ratio, isolation, and crosstalk in addition to bandwidth. Throughout the paper, Jhangiani uses equations and figures to show how each of these characteristics affect signals and why they're important.

The **figure** shows how switches can attenuate signals. Assume that the input signal is a 3-GHz sine wave. At that frequency, significant loss can occur. Because attenuation may be nonlinear, you should look at a switch's entire frequency-response curve to find the best switch for your application.

Martin Rowe, Senior Technical Editor

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Agilent Technologies

FIBER-OPTICS TEST

16 for the ROADM

DEVICE UNDER TEST

Reconfigurable optical add-drop multiplexer (ROADM) modules used in dense-wavelength division multiplexing (DWDM) communications networks. The modules mount on network-interface boards, and they can remove a channel destined for a specific network node. The modules operate in the C band (1520–1570 nm) on 45 channels. A ROADM can remove up to eight channels from a DWDM stream and add them back to the network.

THE CHALLENGE

Test and calibrate ROADMs following manufacture to ensure proper optical output power, wavelength, and bandwidth. Test for insertion loss, polarization-dependent loss, and chromatic dispersion under controlled temperature conditions. Perform tests on up to 16 ROADMs at once.

THE TOOLS

- Agilent Technologies: swept-wavelength test system. www.tm.agilent.com.
- JDSU: swept-wavelength test system, optical switches. www.jdsu.com.
- Luna Technologies: optical vector analyzer, optical switches. www.lunatechnologies.com.
- Tenney: computer-controlled temperature chamber. www.tenney.com.

PROJECT DESCRIPTION

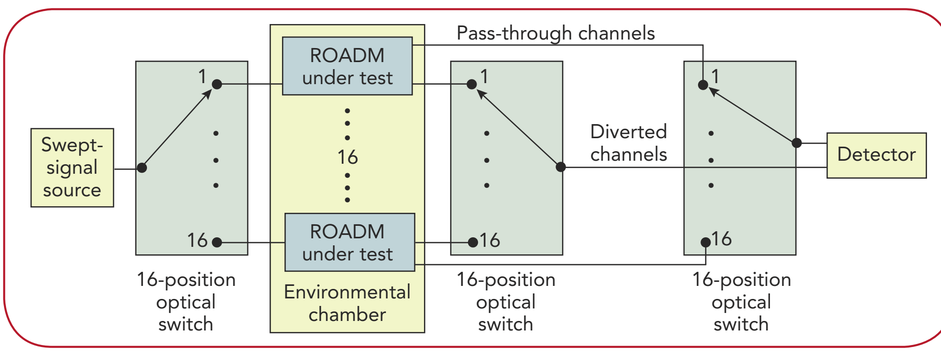
Nistica (Bridgewater, NJ; www.nistica.com) designs and manufactures ROADMs used in telecom switches produced by several manufacturers. Telecom carriers use ROADMs in the switches to divert DWDM channels to network nodes. A ROADM mounts on a network-interface board that controls the module through an RS-232 or I²C port.

A ROADM is essentially a tunable notch filter that removes a channel from a DWDM stream and diverts it to a network node. It can also add channels back into the stream. Each channel is approximately 800 pm in wavelength; a ROADM must remove a channel from the stream without affecting remaining channels. Nistica tests and calibrates each ROADM to ensure that its output—the diverted as well as the pass-though channels—operates at wavelengths and power levels that are compatible with network equipment.

Nistica's production test stations consist of optical switches and a swept-wavelength test system, which includes a swept-signal source and a detector (**figure**). The optical source sweeps through the C band, while the detector measures power, wavelength, insertion loss, and group delay in 3-pm increments. The calibration process produces calibration factors for the ROADM that adjust its optical output for wavelength and power. Optical switches let the system test and calibrate up to 16 ROADMs at a time.

At the start of each test, a technician inserts a piece of optical fiber into the circuit, creating an optical "short circuit." The optical source sweeps through the C band, producing light at a known optical power. The detector measures the power every 3 pm, producing a set of reference values as a function of wavelength. Then, the technician removes the fibers and inserts the ROADMs into place. A repeat measurement reveals the difference: insertion loss, which can be as high as 90 dB before calibration. The system also measures group delay at each wavelength.

During a calibration, the test system controls the device under test's (DUT's) input-signal power as it sweeps across the C band and measures the output power of the removed and adjacent channels at 3-pm increments. Calibration occurs with the DUT in an oven at a known temperature ranging from –5°C to +65°C. Having acquired data at each wavelength, the system calculates calibration constants that correct the ROADM's output power and wavelength. Calibration aligns the ROADM's channel wavelengths to those expected by other network equipment. The system then stores each ROADM's calibration constants in the appropriate ROADM.



A production test system for reconfigurable optical add-drop multiplexer (ROADM) modules tests and calibrates each module for wavelength and output power.

LESSONS LEARNED

"Tracking of the swept input signal is critical," said Nistica CTO Tom Strasser. "3 pm is the practical wavelength limit of the test equipment in terms of resolution." The system spends 10 s at each measurement point, and with measurements performed at 3-pm increments, there are about 25,000 sets of measurements across the C band. Strasser also pointed out that calibration is important to ensure that a ROADM sufficiently removes a DWDM channel with minimal effect on adjacent channels.

Martin Rowe, Senior Technical Editor

VOTE *for the* 2008

OUR EDITORS SELECTED SIX FINALISTS FOR THIS ANNUAL AWARD.

To help choose the winner, cast your ballot by December 5.

The responsibility for ensuring the quality and reliability of electronics products falls squarely on the shoulders of test engineers, whose work touches every stage of a product's life as well as every component that makes up a product. In the lab, in the factory, and in the field, test engineers weed out faults that can lead to poor products and can sully the reputations of companies and even countries.

To acknowledge this essential role of test engineers, *Test & Measurement World* announces its fifth annual Test Engineer of the Year competition. Thanks to the contributions of the award sponsors—Keithley Instruments and National Instruments—the winning candidate will designate a $20,000 donation to an engineering school.

Test & Measurement World will present the 2008 Test Engineer of the Year award at our annual "Best in Test" ceremony scheduled to be held in conjunction with the 2008 APEX Show (April 1–3, Las Vegas, NV). In addition, we will profile the winning engineer in the cover story of our April 2008 issue.

In recent weeks, we've received many nominations of outstanding test engineers from a broad range of fields. Our editors have selected the six individuals presented here as the finalists for the award. Please review their profiles both for on-the-job skills and for overall contributions to the test field and the industries they serve. Then, cast your vote online by visiting www.tmworld.com/teoty, where you will find additional links to information on the candidates and their companies. We must receive your vote by December 5, 2007.

DEADLINE: DECEMBER 5, 2007

WWW.TMWORLD.COM/TEOTY

BOARD TEST

James J. Grealish

Intel

WITH MORE THAN 25 YEARS IN BOARD TEST, JAMES "JJ" GREALISH HAS WORKED on important disk drive projects for Western Digital and computer motherboards for Apple. For the last 12 years, he has served as senior board test technologist with Intel's Test Development Engineering group in Portland, OR, where he is responsible for looking at the roadmap for board test, identifying potential problems, and working toward solutions.

"In 2006, I gave a presentation at the International Test Conference, outlining the growing problems with test access as motherboards become more and more dense," recalled Grealish. In no small part, that presentation led to a cooperative effort between Intel and Agilent Technologies to spread the use of Agilent Bead Probes in high-volume in-circuit test. This technology places solder beads or "bead probes" directly onto PCB signal traces, a technique that cuts manufacturing costs by eliminating rerouting of signal paths during board layout to accommodate traditional test pads.

Several OEMs have already adopted the technique, which Grealish believes will extend the viability of in-circuit test for years to come. He now spends time educating other engineers on how to implement the new technology.

MEDICAL

Steve Kobs

GE Healthcare

EVERY DAY, HOSPITAL MEDICAL STAFFS MAKE CRITICAL DECISIONS BASED ON data collected and displayed on bedside patient-monitoring devices. It goes without saying that the reliability of such equipment is essential.

At GE Healthcare, Steve Kobs led the engineering team responsible for designing an automated manufacturing test system for the company's latest data-acquisition product for monitoring, the CARESCAPE patient data module (PDM). This device, about the size of a paperback book, collects and processes parametric information on vital signs such as blood pressure, blood oxygen levels, respiration, temperature, and cardiac output.

Kobs and his colleagues designed a "one touch" test system that incorporates an interface between the bundle of parametric cables and the device under test, allowing for a single insertion and automated ejection. In conjunction with a patient simulator designed by Kobs, the fixture also tests the PDM's ability to recognize and communicate with "smart" cables connected to it.

Among other advances, the fixture pioneered "forced maintenance" features that Kobs says will be used on testers for other products. These include automatic lock-down of equipment for maintenance after a prescribed number of tests have been performed, a strategy that helps eliminate test-induced failures.

TEST ENGINEER of the YEAR

FAILURE ANALYSIS

Pat McGinnis

IBM

"WHEN STANDARD TESTS AND DIAGNOSTICS CAN'T ISOLATE FAILS, THAT'S where I come in," said Pat McGinnis of his troubleshooter role at IBM's Systems and Technology group, where he heads an engineering team in a pivotal diagnostics lab.

McGinnis and his colleagues have performed structural and functional tests, as well as image diagnostics, on dozens of high-profile chips. These include: the latest dual-core IBM Power6 processor, the STI (Sony, Toshiba, IBM) Cell processor, the Xbox 360 game chip, and the Nintendo PowerPC game processors. The team has also conducted key fault localization for 45-nm, 32-nm, and LP (low power) process functional test macros.

McGinnis stressed the importance of targeting the product and the process simultaneously. As demand for his lab's services grows, his toughest job is to find and train engineers skilled in using both automated test equipment and sophisticated failure-analysis tools, such as laser scanning and photo emission microscopes and picosecond imaging circuit analysis (PICA) tools.

But the rewards can be huge. "We've fixed problems that impacted yields as much as 60 to 70%," said McGinnis. "This work can affect business in a very high-dollar way."

MICROWAVE TEST

Hung Nguyen

Raytheon

DR. HUNG NGUYEN, RAYTHEON'S CHIEF SCIENTIST, HAS SPENT MORE than 20 years designing, integrating, and testing advanced airborne radar systems. Hung's role as a premier problem solver begins when a radar system's hardware and software are integrated in the lab. And it carries through with tests when the radar is mated with the mission-control computer and avionics during flight testing. Even after a system is handed off to production, Nguyen is on call if manufacturing tests turn up problems. Finally, he sits in on design reviews to apply lessons learned from his work on four pivotal radar systems.

Much is at stake. "With the millisecond response times required in military operations, our tests must ensure that radar is free of any anomalies," explained Hung. "We need to test the system not only to verify what it is supposed to do, but also to raise questions when it's doing what it's not supposed to do."

In Raytheon's new APG-79 system, now being deployed on the Navy's F18 fighters, Hung and his test colleagues had to ensure reliability of a complete redesign of the receiver/exciter, the processing system, and the antenna, which features a fixed array with active electronic beam scanning. The payoff for Raytheon: a multiyear, $580 million contract.

SOC/RF TEST

Richard Stilwell

Analog Devices

AS MEDICAL ULTRASOUND SYSTEMS ARE PACKAGED INTO EVER-SMALLER instruments, they no longer have enough real estate to accommodate image-acquisition technology that uses multiple components and ICs. Analog Devices has met the needs of such applications with its AD9271, an eight-channel system-on-chip (SOC) device that combines a low-noise amplifier, a variable-gain amplifier, an anti-aliasing filter, and a 12-bit analog-to-digital converter. Compared to discrete elements, the AD9271 reduces the area per channel by more than one third.

Combining these functions in an SOC for ultrasound presented tough test challenges, and it fell to Richard Stilwell, staff test development engineer, to find a test platform capable of testing all the functions simultaneously. His choice: the LTX Fusion, which delivered test times half that of the nearest competitors.

For such SOC applications, Stilwell noted that it is essential for test engineers to have a thorough understanding of the end product and its operation. "This requires a much greater system knowledge," said Stilwell, whose work has set the stage for testing future system-level chips in an economical fashion.

AEROSPACE TEST

Craig Stoldt

Manufacturing Technology

WHAT DO YOU DO WHEN EXPENSIVE MILITARY TEST EQUIPMENT THREATENS to become inoperable, as the government extends the operational life of aircraft beyond the ability of vendors to support aging ATE systems? You call on engineering manager Craig Stoldt, whose employer—Manufacturing Technology—is a leader in a field called "obsolescence mitigation."

With more than 35 years of ATE experience, Stoldt has become an expert in breathing new life into legacy systems by finding both hardware and software fixes that can emulate the original technology. "Our work takes a lot of reverse-engineering skills," noted Stoldt, "and the goal is always to make the test interfaces look the same to those who do the testing."

Cost controls are a prime consideration. "We're always asking how we can reuse what is still functional," he explained. "In some systems, hundreds of test programs have been devised, and we want to make sure that we can use as many of them as possible in our upgraded ATE design." With such strategies, Manufacturing Technology has saved its military clients many millions of dollars.

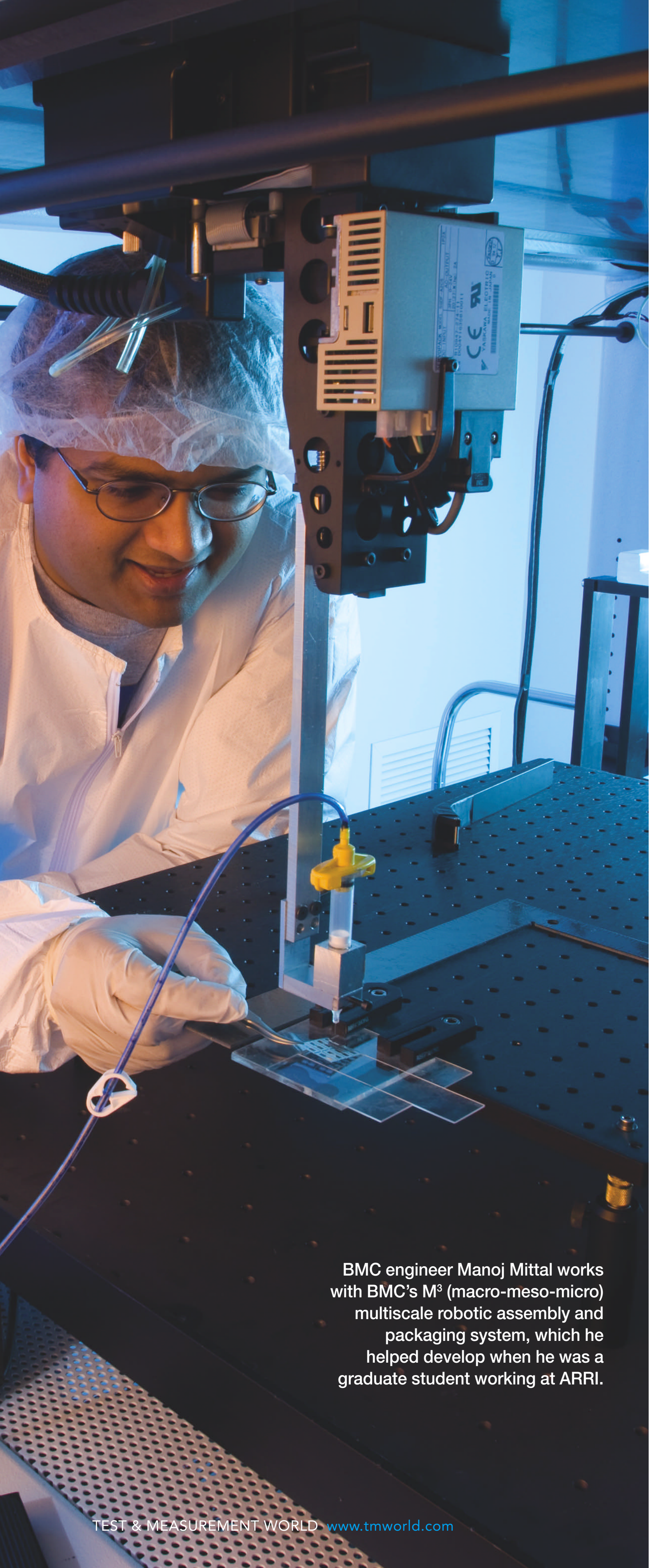
Aside from his job, Stoldt remains active as a teacher, instructing other engineers on ATE, test-program development, and ATLAS, a military test-programming language. T&MW

TAKING MEMS SENSORS TO MARKET

The Bennington Microtechnology Center, in conjunction with its academic partner, develops the processes that bring MEMS devices from concept to commercialization.

BY RICK NELSON, CHIEF EDITOR

Henry Klim, executive director of the Bennington Microtechnology Center, and Dr. Harry Stephanou, director of the Automation & Robotics Research Institute at the University of Texas at Arlington and BMC founder and chairman, collaborate on MEMS design, production, and test.



BMC engineer Manoj Mittal works with BMC's M^3 (macro-meso-micro) multiscale robotic assembly and packaging system, which he helped develop when he was a graduate student working at ARRI.

NORTH BENNINGTON, VT. The burgeoning microelectromechanical systems (MEMS) field is full of good ideas, as researchers pursue innovations ranging from smart-weapon components to miniature medical devices. But turning good ideas into products that can be manufactured and tested in quantity can be difficult. To address the production and test challenges, the Bennington Microtechnology Center (BMC) was founded in 2004 to provide assembly, packaging, and test solutions for MEMS devices used in biotech, military, commercial, and industrial applications.

BMC works with its academic partner, the Automation & Robotics Research Institute (ARRI) at the University of Texas at Arlington, to provide services that range from concept creation to full production, said BMC's executive director Henry Klim, in an interview at the organization's facility here. Dr. Harry Stephanou, ARRI's director, who is also BMC founder and chairman, said in a phone interview that an impetus for founding BMC was the need for an organization that could go beyond the prototyping capabilities of a university laboratory to provide pilot and low-volume production runs.

Founded with congressional funding championed by Vermont's US Senator Patrick Leahy, BMC's first customer was the US Navy, for which BMC builds safe-and-arm devices, which monitor environmental inputs to control the deployment of weapons systems. Used on a torpedo, for example, a safe-and-arm device can detect acceleration due to launch from a vessel and disable its safe mode; it then arms itself on encountering deceleration when contacting a target.

Targeting biotech and commercial markets

Klim, who joined BMC in the summer of 2006, said that he is now working to move the firm into biotech and commercial markets as well as military ones. In conjunction with ARRI, the organization is developing devices and processes for inertial, optical, and RF applications. BMC now occupies 12,000 ft^2, including a 3000-ft^2 class 10,000 clean room.

Klim said there are a number of places in which a customer can take advantage of BMC's capabilities.

PHOTOS: AL FERREIRA

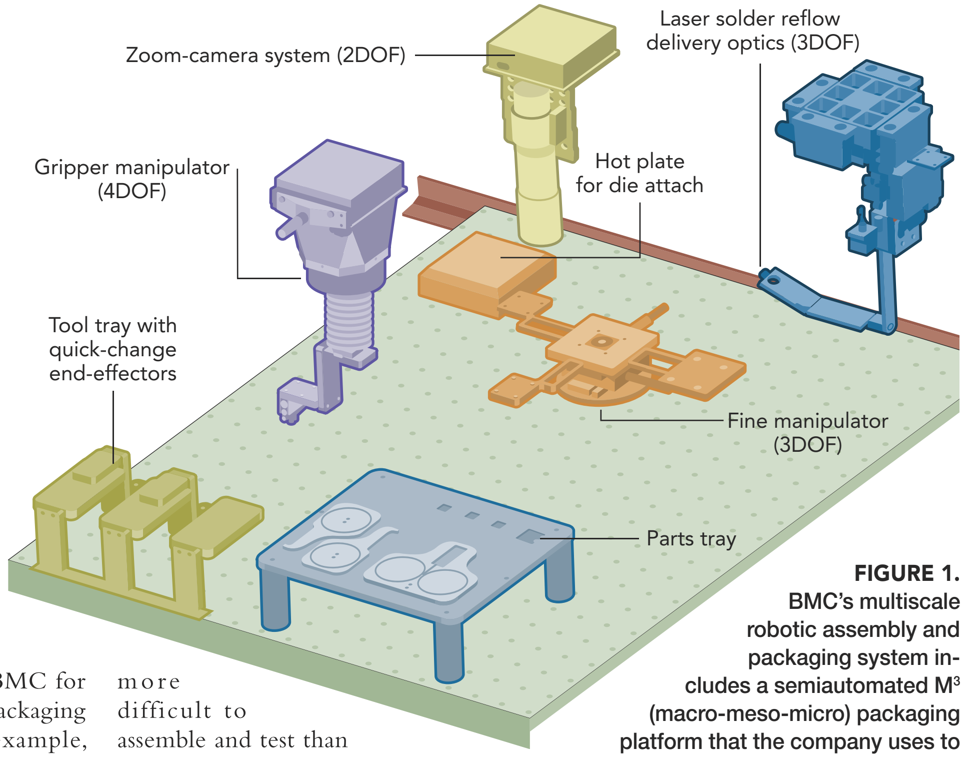


FIGURE 1. BMC's multiscale robotic assembly and packaging system includes a semiautomated M^3 (macro-meso-micro) packaging platform that the company uses to develop modular automated processes.

For instance, a client who has fabricated hermetically sealed packages may want to contract for BMC to verify that the packages are properly sealed using BMC's Norcom 2020 optical leak tester. Other test-specific equipment available at BMC includes a Veeco Wyko 3-D surface profiler, which can perform static surface characterization and dynamic testing of MEMS devices; a Trio-Tech bubble tester, for gross leak testing of package seals; a Suss MicroTec manual wafer prober, for functional testing of MEMS dies; an Instron Microtester pull tester, for wire-bond testing; and an Olympus BH2 microscope, for optical sample inspection.

Other clients may turn to BMC for one stage of an assembly and packaging process. One customer, for example, takes advantage of BMC's Kulicke & Soffa ball bonder to make I/O connections to an imaging chip.

Such projects develop revenue for BMC, providing employment opportunities for equipment operators and helping BMC meet its economic development goals. But the sweet spot for the client, Klim said, is to come in at the beginning and take advantage of the combined capabilities of ARRI and BMC in bringing a concept to fruition.

ARRI's primary domain is in concept creation and design analysis, Klim said, with BMC taking the lead in process development and production. But the two organizations cooperate throughout the entire process, from concept creation and design analysis, through process design and development, and on to production, quality assurance, delivery, and supply-chain management. Stephanou pointed out that although BMC serves as a client's primary point of contact, the interaction between BMC and ARRI is seamless, so clients don't have to worry about the organizations pointing fingers at each other.

Typically, Klim said, an inventor will come in with one device he has made in his laboratory, and now he wants to make a hundred. And often, added Stephanou, the original design makes the product more difficult to assemble and test than is necessary. In such cases, BMC and ARRI can make design recommendations with regard to manufacturability and testability, and they can also help address basic functionality decisions.

For example, a customer might propose to power a device using batteries, when energy harvesting might be a viable approach. By enlisting BMC and its ARRI partner, Klim said, a customer can get the benefits of experts who are working on a fivefold improvement in energy-harvesting efficiency.

Bridging the valley of death

Commenting further on BMC and ARRI interaction, Stephanou said, "We bridge the proverbial valley of death," which often swallows up technologies developed at university labs before companies can convert them to marketable products. The key, he said, is to address not just products but rather the assembly and packaging techniques as well as the equipment necessary to manufacture them. Further, ARRI and BMC address product, process, and equipment development in ways compatible with their respective organizational strengths.

BMC, Stephanou said, is positioned to react to clients' immediate needs: "BMC must be competitive and have a fairly short planning horizon to meet the expectations of clients who always want something yesterday." In contrast, he said, "at ARRI, the job is to look a few years down the road and to try to extrapolate from what clients want today and anticipate what they will want in the future, with respect to the products they will want to build as well as the processes and equipment they will need to build those products. ARRI pursues the disruptive technologies that carry a high degree of risk. If you are running a company, risk is typically not a good thing, but for ARRI, risk is a good thing."

Traditionally, Stephanou said, MEMS manufacturers tend to use legacy equipment—designed for microelectronics—that's expensive and not flexible enough to be effective for manufacturing the variety of MEMS devices that are emerging. In fact, the *raison d'être* for BMC, he said, is to serve the fragmented MEMS market with the ability to cost effectively and reliably handle small production runs. "Anybody can automate a process to make trillions," he said, "but the challenge is to make small batches." The key, he said, is modular equipment that can operate at multiple scales—meters, centimeters, microns, and nanometers. *(continued)*

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Agilent Technologies

Test focus shifts to MEMS

HOPKINTON, MA. "With MEMS sensors, we are testing at the extremes of environmental stimulus and response while simultaneously being involved with I/O, data conversion, and signal processing," said Tom Farkas, president and founder of Metrikos, adding, "It's the messiest, ugliest kind of test you could ever possibly do." And that suits Farkas just fine, who is ready for new test challenges.

"In the '80s, microprocessor test was the key driver in the ATE industry, and in the '90s, the driver became wireless," explained Farkas, who was involved in wireless test as a cofounder of StepTech, a maker of RF instrumentation that LTX acquired in 2003. Today, he said, the focus is shifting to test of devices that acquire environmental or other external nondigital information.

Farkas provided an example of how manufacturers would traditionally deal with such information. They might fabricate bimetallic strips for use in thermostats. The vendors would sometimes batch-test the strips and very rarely calibrate them. With one thermostat per room or floor, users could simply manually adjust them to compensate for lack of calibration.

The situation is quite different now, Farkas said: "Imagine a green-building application with fully automated HVAC. That application might involve distributing thousands of Zigbee-empowered humidity and temperature sensors throughout a skyscraper. They will all need to be tested and calibrated in high-volume manufacturing environments."

Adding the wireless element, he said, further complicates the test task: "You've got this module that you have to test, and it's environmental stimulus in and bits out, and the bits may come out not on a piece of copper but at 2.4 GHz. It's not the sort of thing where you can directly apply the old chip-test regime."

A partnership with BMC, announced last June, gives Metrikos an opportunity to determine the direction of the new MEMS-test regime. "BMC is in the forefront of developing the processes that will enable the assembly and test of these new devices, which are not individual, integrated pieces of CMOS but rather multiple device types—including sensors, radios, and energy harvesters—that must be assembled in stacked-die, system-in-package, or other complex configurations. You can't just assemble something high-value like that and then expect it to pass a single, final functional test. You have to test it as you are building it." Working with BMC, Farkas plans to be on the forefront of developing test techniques that will be extensible to large-scale production.—*Rick Nelson*

Said Klim, "We are not selling commodities. Our business is the development, assembly, and packaging of odd and unusual devices. The vast majority of our work is done developing processes." And that work, he said, involves significant input from ARRI. "Our alignment with ARRI makes a lot of sense," he added. "They are developing robots that in turn build series of successively smaller robots."

Klim said ARRI's approach melds well with BMC's concept of modular automation: "We have large robots with a wide range of motion but fairly course resolution as well as smaller ones that have restricted movement but very fine resolution. Our goal is not to have a robot complete one task and then launch another, but rather to dedicate an island of modular automation to each task." That approach, with manual intervention handling the transfer between modules of automation, serves BMC well in its role of a prototype foundry making hundreds or thousands of devices, he said.

Implementing modular automation

BMC's approach is based on the M^3 (macro-meso-micro) multiscale robotic assembly and packaging system, developed at ARRI by Dr. Dan Popa and BMC engineer Manoj Mittal when he was a graduate student working at ARRI. Process development usually begins with a small semiautomated reconfigurable platform (**Figure 1**). When the process is proven, it is transferred to the company's Motoman automated robot system. BMC can provide positioning accuracies to within 1 to 5 microns by dead reckoning and can do better with optical feedback, Klim said.

Such robots help BMC engineers automate many assembly processes, ranging from those involving individual packages to those fabricated using wafer-scale techniques. An example of the latter is BMC's work on a dual-optical-microphone device.

At each stage of the process, BMC ensures quality by implementing what Klim calls "in-process test gates."

The original concept called for assembly of the individual glass and silicon devices, which entailed significant handling problems. As an alternative, Klim said he investigated wafer-scale processing in which the devices' nine layers of silicon structures are built up on a 4-in. glass substrate; singulation occurs after fabrication is complete.

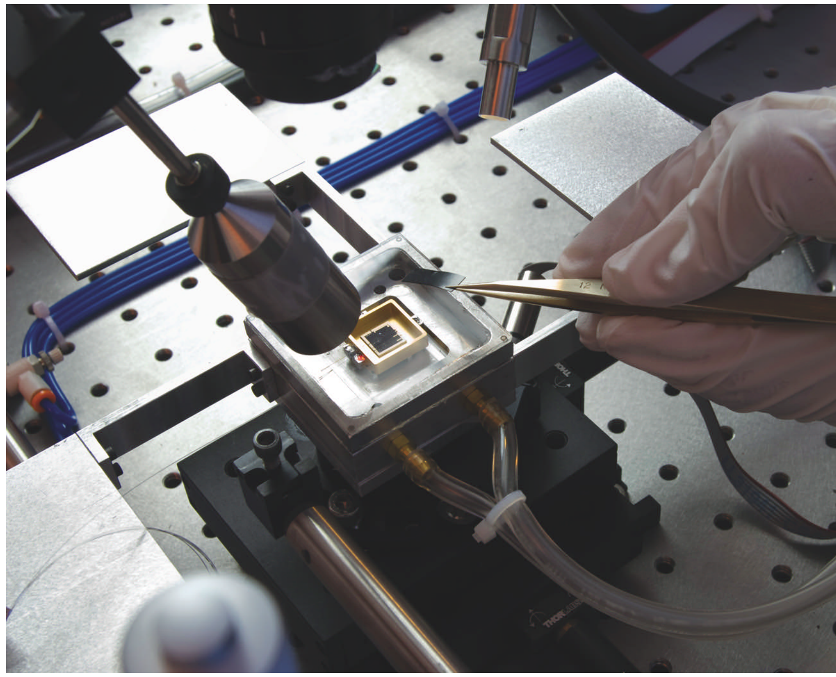
That process presented its own challenges. One was maintaining sufficient flatness and proper alignment as multiple layers are built up on the glass substrate. Another was finding a way to dice a wafer consisting of nine layers of dissimilar materials. "If you want to stack up nine layers and are off by 12 degrees from bottom to top, you're not going to have many good parts after you dice them," Klim said.

The dicing problem was relatively straightforward. "I knew that people are doing a lot of wafer stacking, so I realized, 'somebody has already solved this problem.' I did some research and learned what special saws and surfactant materials we could use to reduce chipping."

As for flatness measurements, when an engineer proposed a dial gauge, Klim insisted he find one with a USB port so the process could be automated. Engineers are good at solving problems, Klim said, but he added that he wants to make sure each problem is solved just once. "If a dial gauge is the answer, then I want it mounted on one of our automated positioning devices, and I want the results sent to a computer. If another engineer comes in, I don't want him to have to relearn how to use the dial gauge. I want every problem solved once. It's a lot harder, initially, to do this up front, but it's necessary. Our processes need to be personnel-independent."

Test gates qualify processes

At each stage of the process, BMC ensures quality by implementing what Klim calls "in-process test gates," each of which must be passed before beginning


AL FERREIRA

A BMC engineer works with a device being fabricated on BMC's semi-automated robotic system.

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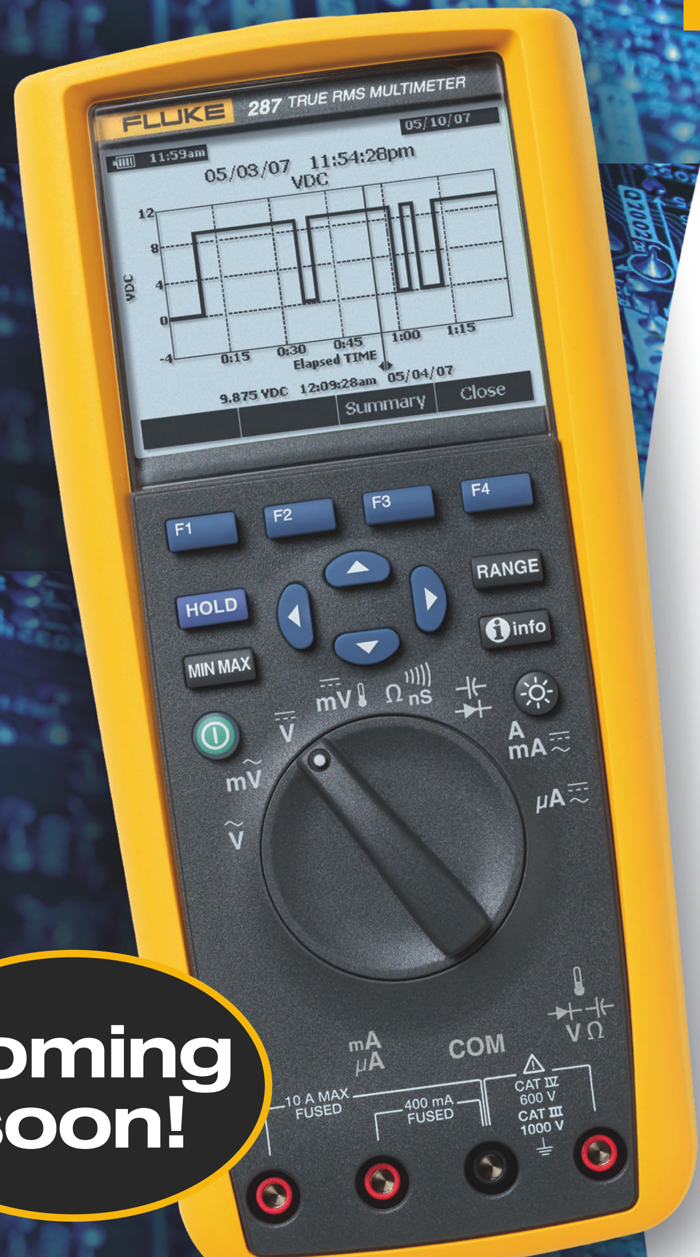

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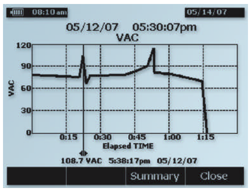

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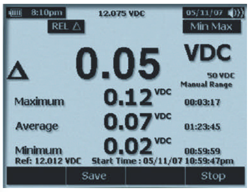

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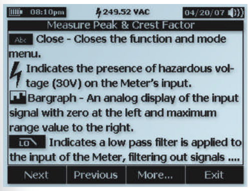

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the next process stage. "We have to qualify the process somehow, and the best way to do that is to have in-process gates where we make measurements. You don't go through that gate unless you have passed some testing criteria; then you go on to the next process step. The concept is simple, but the implementation of these gates can be painful. You have to put a lot of thought into it."

One example of a test gate is the flatness measurement in the multilayer, wafer-scale optical microphone process. Another is the wafer probing used to functionally test MEMS dies before packaging them.

Much of the test that takes place at BMC is destructive, involving bond-pulling and shear tests. "We want to pull wires to make sure they are bonding correctly, and we have a shear machine that we use to twist components we've glued together to see how strong that bond is."

One test aspect that hasn't been emphasized at BMC is final functional test. "The first question I asked when I arrived here is, 'you assemble parts and send them to customers and don't know if they work?'" said Klim. BMC's parts *do* work, because they have successfully passed through the in-process test gates. Klim explained, "The theory is, if you put in enough gates you'll have 100% yield." Further, he said, functional test is not something customers have demanded. Despite that, Klim is looking to an increased emphasis on final functional test, for both BMC's and its customers' benefit. "There is significant value in acquiring physical test data from functioning devices," he said.

To get that data, BMC is investing in a PXI-based test system to be supplied by Metrikos (see "Test focus shifts to MEMS," p. 30). At Sensors Expo in June, BMC and Metrikos demonstrated a preliminary version of the system performing a closed-loop optical-alignment application. At the request of BMC's engineering staff, the system will employ LabView, although Klim, a self-described lab rat, said he would prefer a text-based language like LabWindows CVI, since his experience has indicated that the latter may be more suitable for a production environment because its execution is more deterministic.

Going forward, test will be an increasingly important component to BMC's offerings as the organization builds devices such as accelerometers and RF switches for next-generation cell phones. Roger Grace, a consultant who advises BMC, said his research has shown that assembly and test represents anywhere from 50 to 80% of the cost of a device.

"Silicon is cheap," he said, adding, "What BMC is doing here is attacking the highest contribution to sensor cost." Concluded Stephanou, "Testing has involved little more than voodoo in many MEMS applications. Our goal is to replace the voodoo with science." T&MW

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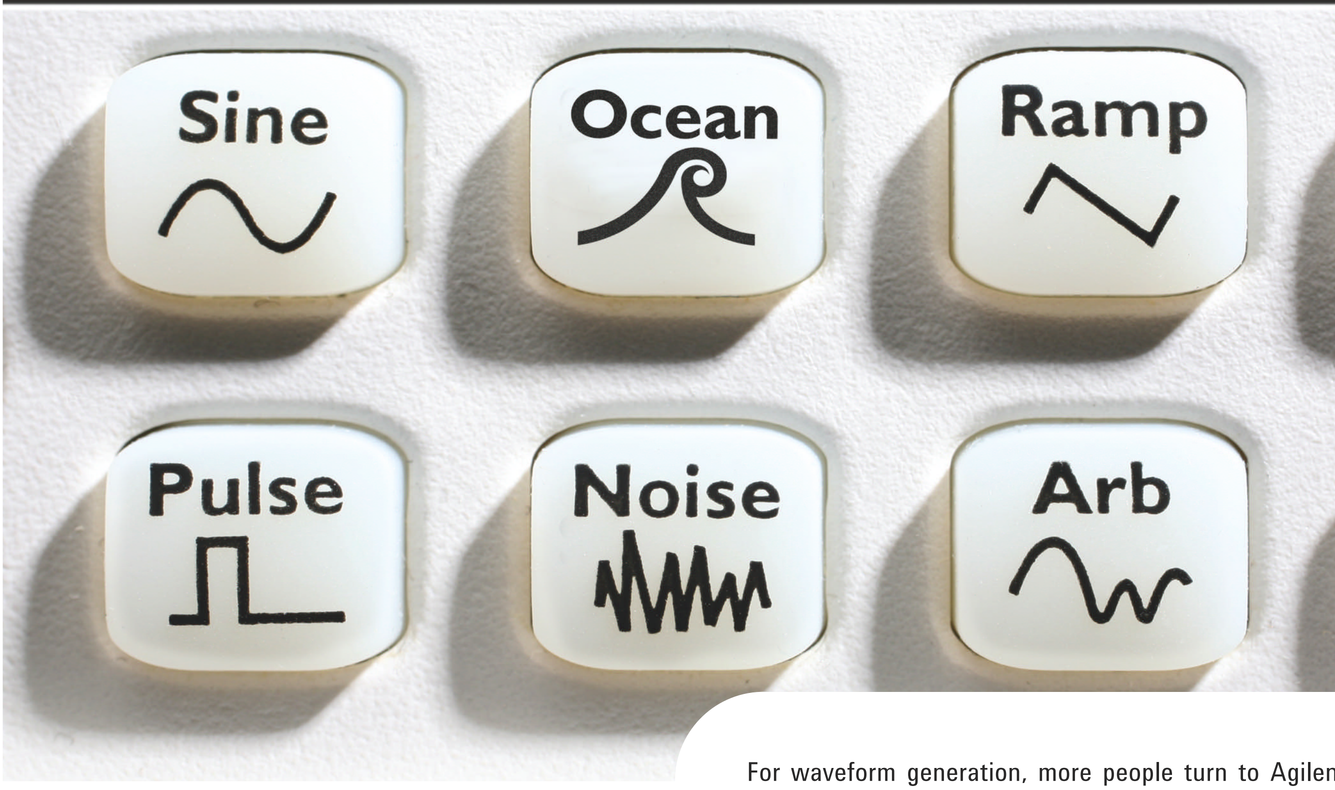

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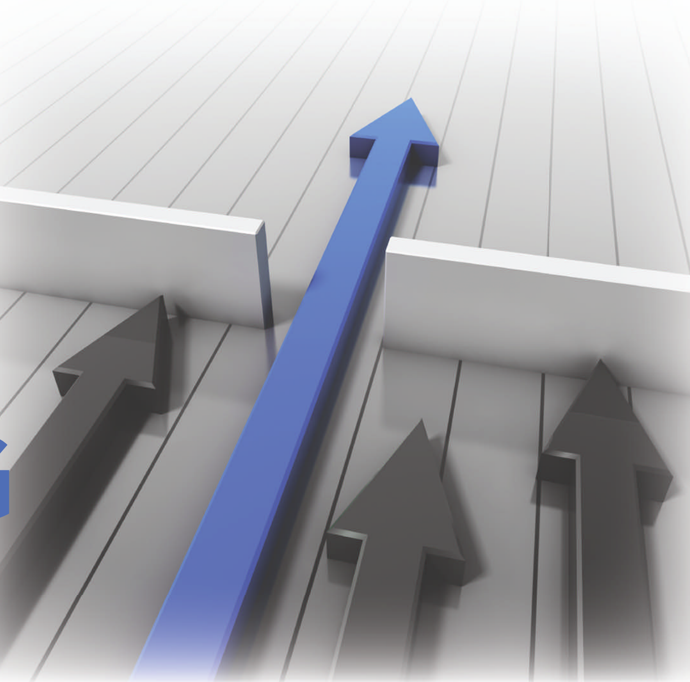


PHASE STEPS OVERCOME SLIM TESTING MARGINS

With a new multiple-strobe technique, your ATE can find the passing setup-and-hold margins during high-volume production test of source-synchronous circuits.

BY STEFAN WALTHER AND GUIDO SCHULZE, VERIGY

With many circuits and systems using clocks faster than 1 GHz, common-phase jitter, drift, and clock skew can affect measurements such as setup-and-hold times. Automated test equipment (ATE) typically strobes clock and data signals with a single strobe with fixed timing that cannot accommodate dynamic phase shifting. To remedy this inadequacy, you can employ a technique that applies a series of strobes—each slightly shifted in phase relative to clocks and data—to accurately test and characterize signals in I/O interfaces such as DDR-SDRAM.

As signal propagation along on-chip interconnects became a limiting factor in device speeds, circuit designers turned to source-synchronous interfaces to alleviate long clock runs. Source-synchronous interfaces receive a master clock and create a local clock for nearby circuits. Local clocks reduce problems caused by power-supply peaks, power and ground noise, local thermal heating, and electromagnetic interference (EMI).

Shifts in a signal's phase can change the circuit timing relative to the ATE, a factor you must keep in mind when testing a source-synchronous interface above 1 Gbps. ("Source-synchronous interfaces," p. 40, explains how the interfaces work.)

Static skew between a local clock and the system clock isn't a difficult problem to overcome. You can use a test method called "output dependent timing" to measure setup-and-hold times. With this method, the test system determines the phase of the transitions in the clock and in the data signals and then sweeps a compare strobe across the timing signals while it monitors the error count. The tester then assigns the correct compare-strobe timing that it keeps for the

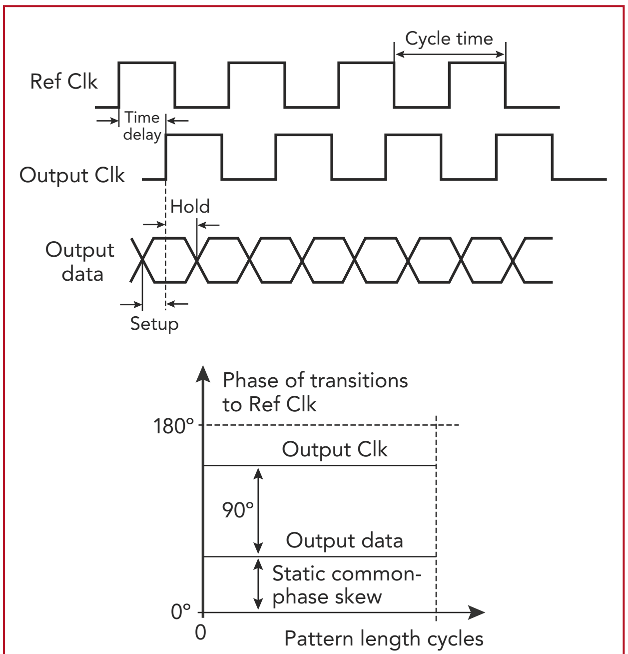


FIGURE 1. In the presence of only static skew to the reference clock, the phase of output clock and data transitions is stable over time.

remaining tests of the device. The phase of the transitions should be stable from bit to bit and shouldn't contain excessive drift or jitter.

Figure 1 shows that for conditions of skew only, the phase of transitions between a reference clock and a source-synchronous circuit's clock remains constant. Thus, an ATE system, which provides the reference clock to the device under test (DUT) during test, can measure setup-and-hold times with a fixed strobe with constant phase relative to the output clock and data.

Above 1 Gbps, drift and jitter can cause the phase of both clock and data to no longer remain constant during the transmission of a data pattern. Thus, the output clock and data lines of a source-synchronous interface (**Figure 2**) will reduce the timing margin associated with a fixed-phase strobe. Because data and clock are synchronized, the phase variations represent a common-phase jitter that won't affect the data transmission.

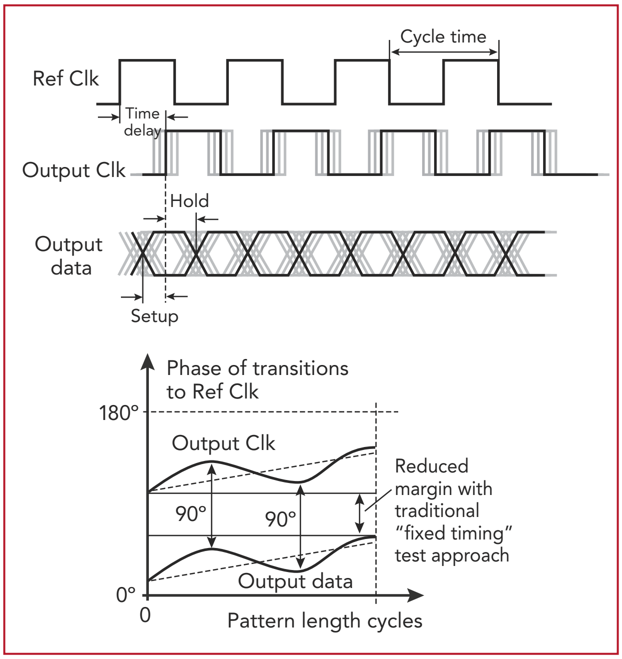


FIGURE 2. In the presence of dynamic common-phase drift and jitter, the phase of output clock and data transitions with respect to the reference clock changes over time, reducing the chance of accurate measurements of setup-and-hold time with a fixed ATE strobing point.

But common-phase drift and jitter will affect measurements if you use a fixed-phase strobe, because when the amplitude of the common-phase jitter is large enough, the moving transitions consume the entire margin, causing failures as soon as the transitions cross the fixed strobe positions. The common-phase drift and jitter cause a data eye to close more than in the device's real application. Therefore, you can't determine parametric (setup time or hold time) data related to the dynamically changing phase of the source-synchronous clock.

Figure 3 highlights the impact of the common-phase jitter. To illustrate the problem, we've rotated the bits counterclockwise by 90° so you can see how the phase of the transition points changes over time. The data's transition points and clock edges track the sine wave that represents jitter amplitude and shape. When the jitter is minimal, the transition points and clock edges will still align with the ATE system's fixed-phase strobe (left-pointing arrows), but timing violations will occur in some bits (indicated by lightning bolts) because of drift and jitter.

To address the timing problem, we've developed a software-based method for testing source-synchronous interfaces even when the common phase shows dynamic variations in drift and jitter.

The method is based on traditional "capture and compare" pin electronics. It scales with the available hardware, and you can easily adapt it for your application.

Our method uses multiple strobes that scan bit cycles to find the points where clocks and data will produce accurate measurements of setup-and-hold time. By scanning the cycles with multiple strobes, you can identify if there is at least one strobe setting that fulfills the setup-time specification of the DUT. Strobe settings in each cycle that don't show errors for the clock or for the data will confirm a valid setup. These error-free strobe settings occur at different phases for each bit cycle N (**Figure 4**). If at least one phase scan step in the cycle passes, then a cycle fulfills the setup-time specification.

In Figure 4, the cycle N–1 yields a pass for strobe settings 2 through 5 on the data-bit line and for strobe settings 1 through 3 on the clock line. Phase steps 2 and 3, where both data and clock lines pass, represent valid test setups. The error-free phase margin for cycle N–1 is one phase step.

For the technique to work, the pattern must repeat and the step width between strobes must be small enough for

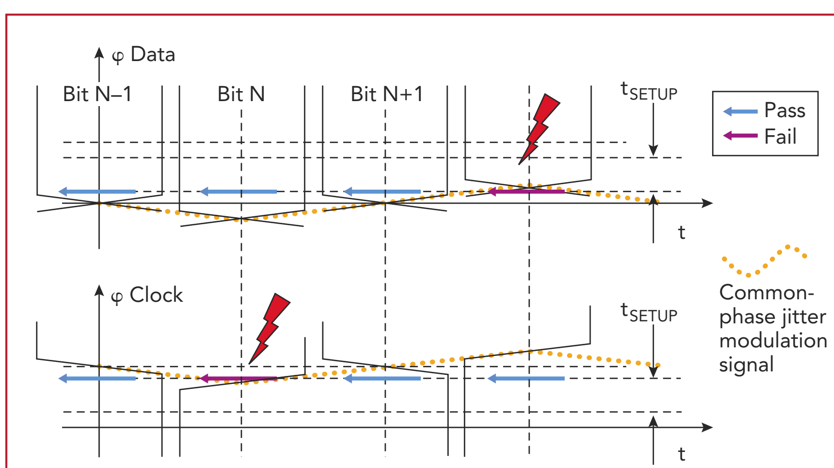


FIGURE 3. Data crossover points and clock edges varying in time because of jitter may not occur at the proper time to be correctly captured by a tester with a fixed timing strobe.

the ATE to find the required points. Even if the distortion varies from one test execution to another, the specified criterion is still valid. You can accept a cycle as passed if it passes with at least one strobe. Because different cycles can pass in different shots, you can accept the whole pattern if every cycle passes in at least one shot.

High-volume testing

Unlike characterization testing, production testing typically doesn't include measurement values. Instead, it uses "pass/fail" testing. The test time for a setup-and-hold time pass/fail verification using our suggested algorithm includes multiple-pattern execution and loading and post-processing of the error data. For cases with long patterns and wide search ranges, the resulting test times are too long for production. To achieve an acceptable test throughput, you need a certain level of ATE hardware support.

You should focus on a few key areas to optimize for high-volume throughput. First, you need the ability to acquire error information per bit at full speed as well as the ability to acquire large amounts of error information within a pattern run.

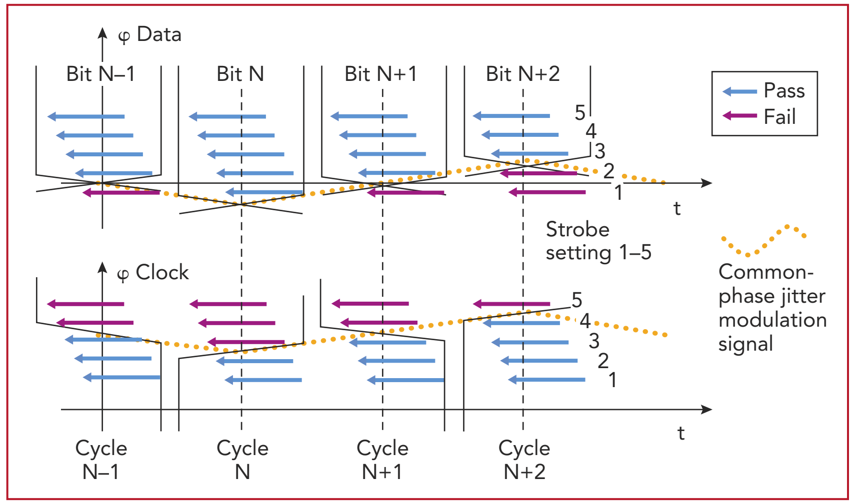


FIGURE 4. Multiple fixed strobes let you find the strobe phase locations that produce valid measurements of setup-and-hold time.

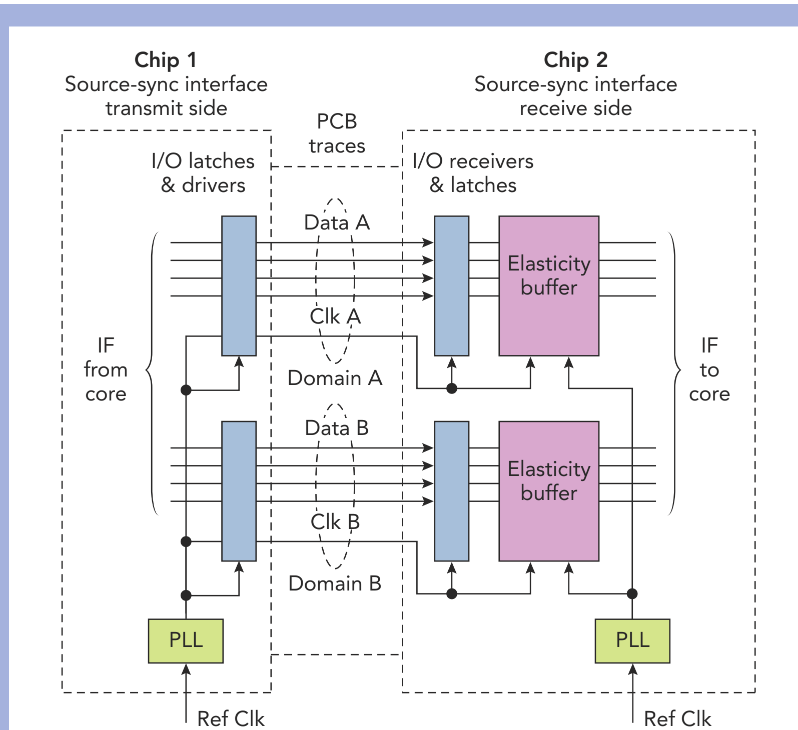
Source-synchronous interfaces

By using stable local clocks derived from a reference clock by means of a phase-locked loop (PLL), circuit designers have sidestepped many of the impairments that on-chip interconnects would introduce in devices with clock speeds greater than 1 GHz. Each local clock, part of a clock domain, services a set of local functions such as I/O interfaces.

The **figure** shows building blocks of a typical high-speed source-synchronous interface connecting two chips for one direction of data transmission. Source-synchronous interfaces are typically split into several clock domains formed by a group of four to eight data lines and an associated source-synchronous clock.

The data and the clock are driven from identical I/O drivers to ensure minimal relative skew and relative jitter between clock and data. On the receive side, the data are latched with the source-synchronous clock. During regular operation, the interface is able to handle common-phase jitter variations up to a certain bandwidth. The purpose of such source-synchronous I/O technology is to increase setup-and-hold-time margins and to enable high-speed synchronous traffic between devices while eliminating the need for precise clock and signal distribution.

Stefan Walther and Guido Schulze



A source-synchronous interface uses PLLs to lock onto a reference clock, producing a local clock domain.

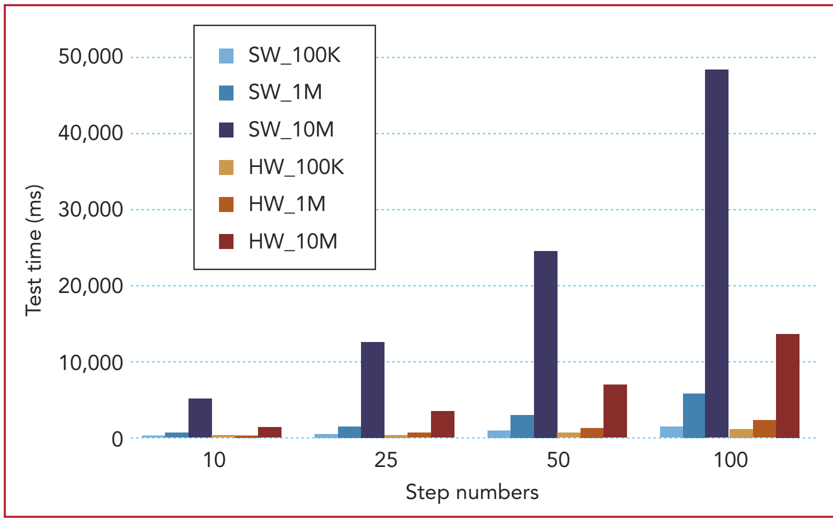


FIGURE 5. Data processed in hardware results in shorter test times.

You must also minimize the amount of data that you need to upload and process.

The Verigy V93000 tester-pin electronics that we used to implement the test method let us perform Boolean operations on the strobe results of the data and clock pins per cycle during upload. This reduced the amount of upload data that finally passed the serial link between the tester and the controller by a factor proportional to the sum of data and clock pins per source-synchronous domain.

An additional option is to avoid the data upload altogether and perform the data processing within the tester hardware, so that just the global pass/fail test results need to be communicated to the tester controller. Performing the post-processing directly in the hardware eliminates the need to upload massive strobe result data and improves throughput by several orders of magnitude.

Figure 5 illustrates the dependency of test time on the number of phase steps and the pattern length of the example source-synchronous interface. As test time translates into cost, a reasonable tradeoff for the test coverage in terms of pattern length and number of phase steps needs to be determined. For characterization, even a pattern that is 10M vectors long with 100 phase steps would give an acceptable test time, when local data processing in the tester hardware is used.

Designed for use with standard ATE, the test methodology we've described is based on traditional capture-and-compare pin electronics. You can scale the technique with your ATE hardware. The test method lets you perform both measurement (characterization) and validation (pass/fail) of timing parameters with fast throughput. You can also perform detailed analysis of failure mechanisms, including waveform shape, amplitude, and spectral content of common-phase drift and jitter. T&MW

FOR FURTHER READING

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Guido Schulze *is a former senior application consultant and now product manager with Verigy's SOC test solutions. He has more than 9 years of experience in test and measurement, first with Hewlett-Packard and then with Agilent Technologies.*

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IPC STANDARD HELPS REDUCE component defects

New specifications and tests for moisture and reflow sensitivity yield more reliable ICs and PCB assemblies.

BY TOM ADAMS, CONSULTANT, AND
STEVEN R. MARTELL, SONOSCAN

The molding materials used to package lead-free components differ from conventional epoxies in two ways: They take up moisture more slowly, and they better resist higher temperatures. But at the higher temperatures needed to melt lead-free solders, a component becomes so hot that almost any entrapped moisture will flash into steam and cause damage. In addition, a large difference between the coefficients of thermal expansion of packaging materials can lead to electrical damage. In each case, damage can range from small delaminations to large visible defects, such as a popcorn crack that extends from below the die paddle to the top surface of the epoxy package (**Figure 1**).

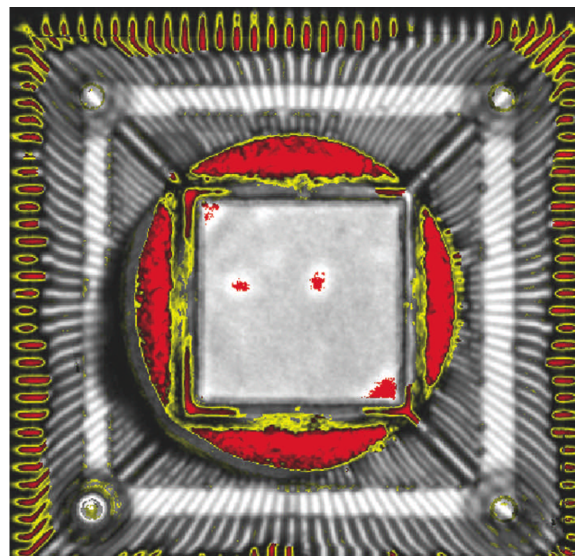


FIGURE 1. **A popcorn crack within a plastic QFP package appears as the red circular area around the die. The assigned color of the crack's edges changes from yellow to black as the crack gets closer to the surface of the device.** Courtesy of Sonoscan.

The new IPC/JEDEC J-STD-020D standard gives manufacturers of electronic components and systems specific defect guidelines and definitions that will help them avoid problems in final products (Ref. 1). The standard, revised in June 2007, provides information so manufacturers can test and classify their components and assign moisture-sensitivity levels to them. These levels help assemblers of printed-circuit boards (PCBs) ensure they apply components to boards and solder them within a specified floor-life time and within reflow-profile restrictions.

During the specified floor-life period, components will not absorb enough moisture to cause problems. The D version of the standard provides a lead-free solder classification reflow profile and specific pre-test soak requirements for the molding compounds that have been formulated to survive the higher temperatures of lead-free reflow. (A reflow profile defines the temperature vs. time exposure for a PCB as it moves through a reflow oven.)

The new standard also supplies test specifications that dictate the environmental conditions that must be used to precondition packaged devices. So, component and system manufacturers start with the same definitions as they tailor their processes to manufacture reliable products.

Determining moisture-sensitivity levels

To determine the moisture-sensitivity levels now embodied in the J-STD-020D standard, researchers exposed surface-mount components to specific environmental conditions, simulated mounting these components on a PCB, and passed the PCB through a reflow oven three times using a specific classification-reflow profile. With an acoustic microscope, the researchers obtained preprocessing and postprocessing images that documented both pre-existing defects and defects that occurred during the processing, such as cracks, delaminations, or voids. Researchers at Intel, IBM, NXP (formerly Philips), Agere, and other semiconductor manufacturers performed the painstaking work that led to the standard.

Manufacturers of ICs can use these same tests to classify their components so PCB assemblers can determine how to handle specific types of ICs. The information in **Table 1**, extracted from the J-STD-020D standard, shows the floor life for components in each of eight moisture-sensitivity levels. The floor-life time refers to the maximum time between removing components from their moisture-barrier packages and passing them through a reflow process. The longer a device sits in a manufacturing environment, the more moisture it can absorb.

For components that comply with J-STD-020D, manufacturers will affix a package label that lists the component's moisture-sensitivity level and the peak package-body temperature that the manufacturer allows. Level 3 components, for example, have a floor life of 168 hrs at conditions up to 30°C at 60% relative humidity (RH). In addition, the floor-life specifications cover devices manufactured with a conventional or a higher-temperature molding compound.

When developing the standard, researchers empirically determined appropriate reflow-profile parameters and soak times that IC vendors and PCB-assembly companies can use to test components they plan to subject to assembly-line conditions. Soak conditions specify exposure times for components at specific temperatures and RH levels prior to testing.

Tests involve baking components to remove all moisture and then "soaking" them at the standard conditions chosen for a level shown in Table 1 under "Soak requirements." Prior to testing, the level 3 components require a soak at 30°C and 60% RH for 192 hrs (+5/–0 hrs). To determine whether the moisture and reflow environment caused defects, you must examine the components before and after exposure to reflow conditions.

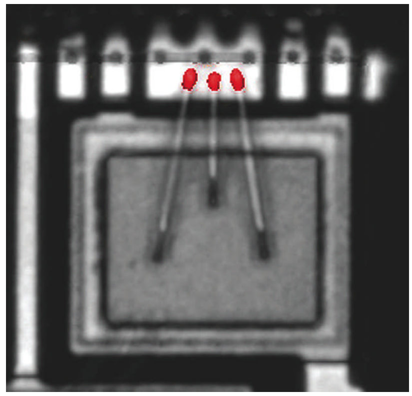


FIGURE 2. The small delaminations (red) at the wire bonds in this acoustic image of a multichip module may cause a failure if the module goes into a product. Courtesy of Sonoscan.

In Table 1, the "Thermal activation energy" columns under the "Accelerated equivalent" heading apply to packaging materials and *not* to solder types. The accelerated equivalents listed in the 0.40–0.48 eV column generally apply to materials used to package devices with lead-based-solder leads. Those listed under 0.30–0.39 eV generally apply to higher-temperature-tolerant materials used to encapsulate devices with lead-free-solder leads.

But in some cases, manufacturers may use the higher-temperature materials with activation energies between 0.30–0.39 eV for components that still rely on lead-based-solder leads. Before you run any tests, make sure you know which materials a manufacturer used to package a component.

Level 3 components, for example, require a standard soak time of 192 hours, as shown in Table 1. If you require a shorter soak time, you can expose typical lead-free level 3 components to a 52-hr soak at 60°C and 60% RH, as shown under the 0.30–0.39 eV heading. Level 3 lead-based components require only a 40-hr accelerated soak at 60°C and 60% RH, as shown under the 0.40–0.48 eV heading. Because molding compounds used for lead-free components take up moisture more slowly than those used for lead-based components, lead-free devices require an accelerated soak time that is roughly 30% longer than that for lead-based devices. At the end of the soak period, you must simulate mounting these components on a PCB, pass the PCB through a reflow oven three times using a specific classification-reflow profile, and then examine components for defects.

Because molding compounds may not have the same moisture-absorption rates, and material suppliers will introduce new encapsulant formulations, we em-

LEVEL	FLOOR LIFE		SOAK REQUIREMENTS				
			STANDARD		ACCELERATED EQUIVALENT		
					THERMAL ACTIVATION ENERGY		CONDITIONS
					0.40–0.48 eV	0.30–0.39 eV	
	TIME	CONDITIONS	TIME (HRS)	CONDITIONS	TIME (HRS)	TIME (HRS)	
1	Unlimited	≤30°C at 85% RH	168 (+5/–0)	85°C at 85% RH	N/A	N/A	N/A
2	1 year	≤30°C at 60% RH	168 (+5/–0)	85°C at 60% RH	N/A	N/A	N/A
2a	4 weeks	≤30°C at 60% RH	696 (+5/–0)	30°C at 60% RH	120 (+1/–0)	168 (+1/–0)	60°C at 60% RH
3	168 hrs	≤30°C at 60% RH	192 (+5/–0)	30°C at 60% RH	40 (+1/–0)	52 (+1/–0)	60°C at 60% RH
4	72 hrs	≤30°C at 60% RH	96 (+2/–0)	30°C at 60% RH	20 (+0.5/–0)	24 (+0.5/–0)	60°C at 60% RH
5	48 hrs	≤30°C at 60% RH	72 (+2/–0)	30°C at 60% RH	15 (+0.5/–0)	20 (+0.5/–0)	60°C at 60% RH
5a	24 hrs	≤30°C at 60% RH	48 (+2/–0)	30°C at 60% RH	10 (+0.5/–0)	13 (+0.5/–0)	60°C at 60% RH
6	TOL	≤30°C at 60% RH	TOL	30°C at 60% RH	N/A	N/A	N/A

Notes:
N/A = not applicable; RH = relative humidity; TOL = time on label

Adapted from IPC/JEDEC J-STD-020D, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

phasize this information paraphrased from a note in the J-STD-020D standard:

Do not use the "accelerated equivalent" soak requirements until research correlates electrical, after-soak, and reflow damage with "standard" soak requirements or if the known activation energy for diffusion of the package materials is not in the range of 0.40–0.48 eV or 0.30–0.39 eV. Accelerated soak times may vary due to the properties of mold compound, encapsulant, and other packaging materials. (The JEDEC document JESD22-A120 provides a method you can use to determine the diffusion coefficient for a material.)

Finding defects

The J-STD-020D standard contains precise defect criteria that define the types of internal packaging defects that could lead to a failure. Specifically, Section 6.1 of the J-STD-020D standard notes that devices that exhibit any of the following are considered failures:

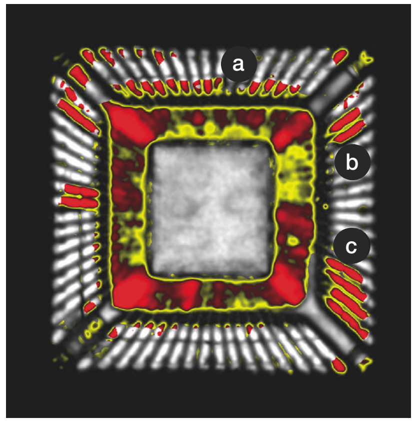


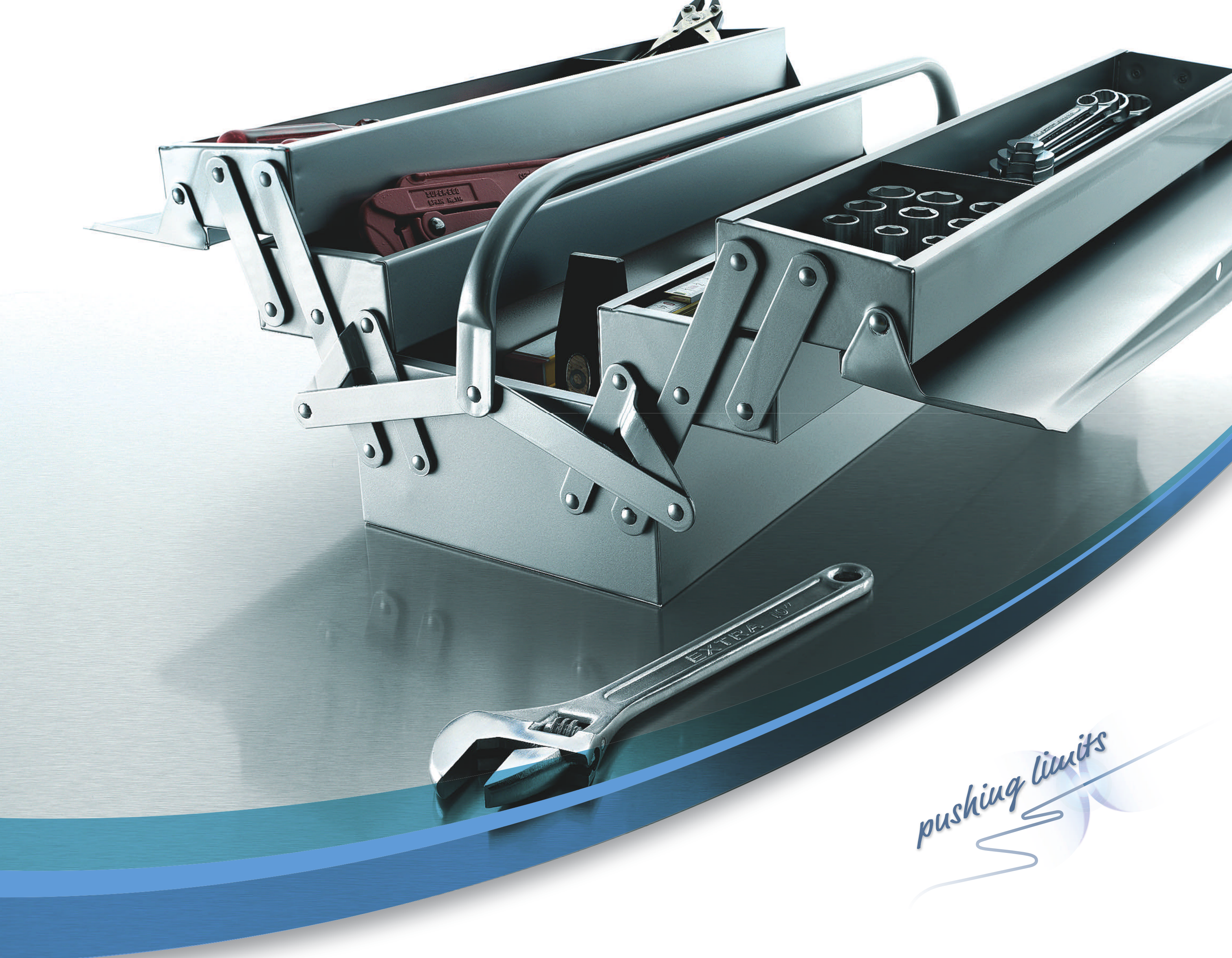
FIGURE 3. This acoustic-microscopy image of a component shows delamination that could break a wire or allow contaminants to reach internal wires.
Courtesy of Sonoscan.

- an external crack visible using a 40X optical microscope,
- an electrical test failure, or
- an internal crack that intersects a bond wire, ball bond, or wedge bond.

Inspection and tests will likely detect the first two types of defects, but devices with subtle internal cracks might pass electrical tests and later cause field failures. Figures 2–4 show the types of defects test engineers could discover either after running specific device tests or during analysis of failed components.

Figure 2 shows an acoustic-microscopy image of components in a multichip module. This type of image uses an assigned color scale to indicate cracks, voids, delaminations, and other changes in the ultrasonic signals used by the microscope. Three wires extend from the die to nearby lead fingers. The red color at the wire ends indicates a crack or delamination where the wires bond to the lead fingers.

Most likely, the molding compound delaminated from the bond area. It is unlikely such small anomalies could cause an electrical failure before final inspection. But these anomalies could eventually cause a wire to break, because of either thermal expansion or moisture-assisted


pushing limits

corrosion. Researchers developed the J-STD-020D specifications to help companies eliminate this type of internal defect.

A component may fail more than one test described in the standard. **Figure 3** shows the acoustic-microscopy image of a cell-phone component. Red and yellow areas immediately around a die usually indicate gap-type anomalies that can have two causes. First, curved wires can scatter the microscope's ultrasound signals and produce an anomaly that does not represent a critical defect. Second, reflections can occur due to delamination of molding compound from the outer edges of the die paddle. This type of delamination defect may be relatively benign.

The red areas—also delaminations—at the inner tips of the lead fingers (Figure 3, area a) and the long delaminations along the length of the top surface of some lead

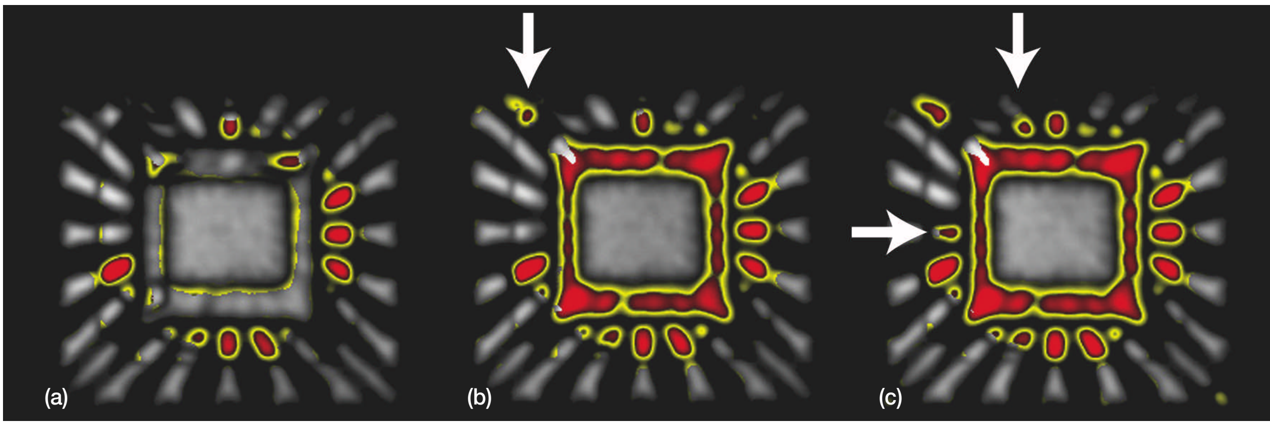
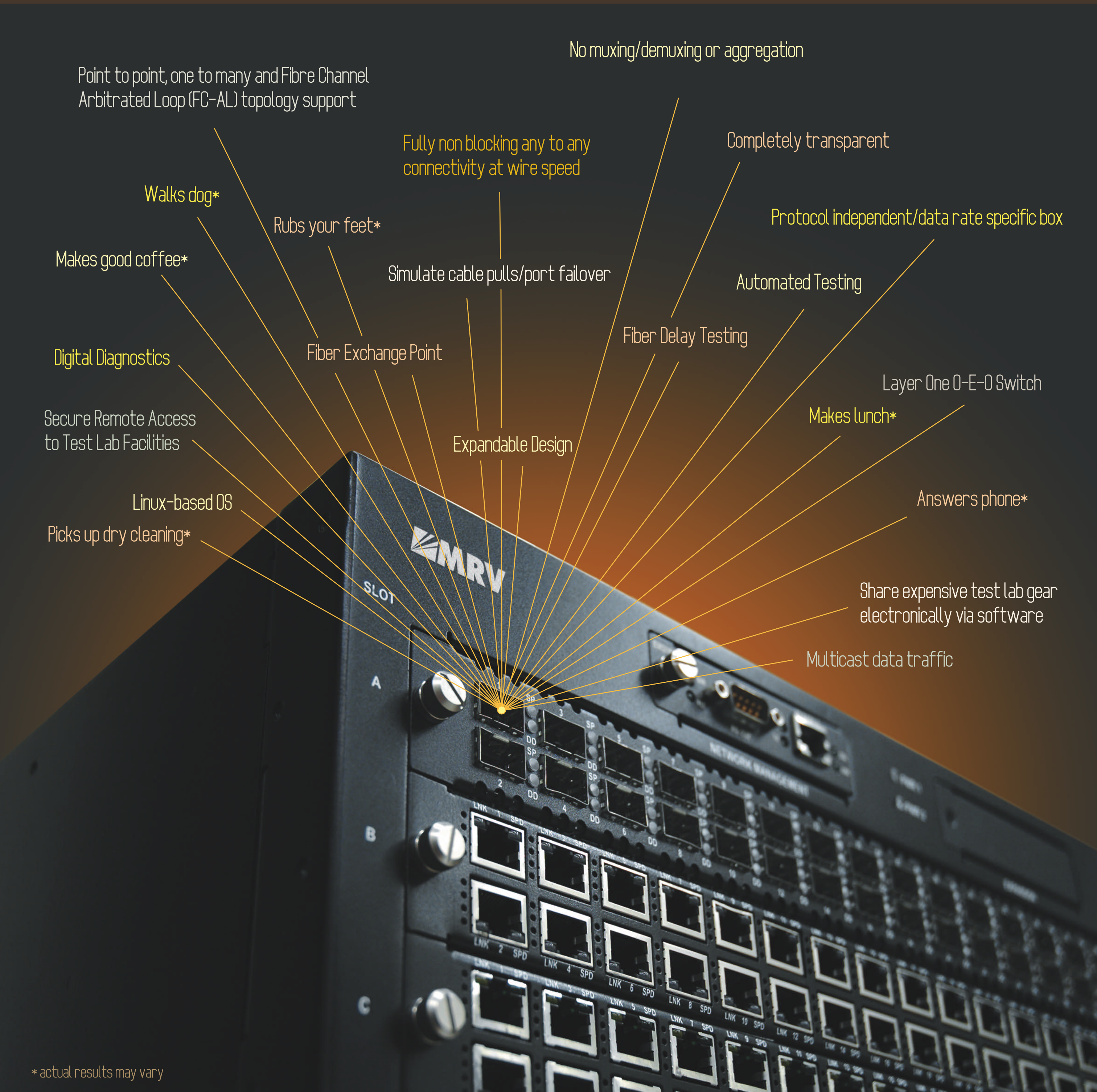


FIGURE 4. This sequence of acoustic images illustrates how internal defects can grow after a chip goes through reflow-soldering processes. The images depict the chip (a) as it was received from its supplier, (b) after 500 cycles of thermal/humidity testing, and (c) after 1000 cycles of thermal/humidity testing. The arrows in b and c point to defects that were revealed during testing. Courtesy of Sonoscan.

At times, nothing could be better than a free port

(Especially when that port can do so much)



Test Automation with a Physical Layer Switch

Media Cross Connect switches are ideal for the Lab Manager and Test Engineer who are trying to create a "light's out" and "wire once" environment. The Media Cross Connect can automate cable reconfigurations in storage systems, servers, peripherals and operating systems. In test labs, the Media Cross Connect offers superior test efficiency and productivity as well as cost performance by allowing test engineers to centralize, share and truly distribute redundant pieces of expensive test gear such as protocol analyzers, traffic/data generators, devices under test (DUT's), servers and storage systems.

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fingers (Figure 3, areas b and c) cause the most concern. These long delaminations require further reliability analysis based on the failure criterion in Section 6.1.e of the J-STD-020D standard, which says that a device cannot have a "surface-breaking" feature delaminated over its entire length. Surface-breaking features include lead fingers, tie bars, heat-spreader alignment features, and heat slugs.

The defects in this component could cause an electrical failure via two possible routes: Delaminations at the inner ends of the lead fingers could break a wire, or one of the long lead-finger delaminations could open a pathway to the exterior and let moisture and contaminants reach the wires.

Not all internal defects cause electrical failures. Some change little or not at all over long periods. But the potential for an electrical failure exists, and manufacturers should not gamble on the future good behavior of internal defects.

The images in **Figure 4** show a component examined with an acoustic microscope at three times. The component began life with several defects (Figure 4a). After 500 cycles (Figure 4b), the defects expanded slightly, the molding compound around the die delaminated, and a new lead finger defect (arrow) appeared. After 1000 cycles (Figure 4c), expansion continued and new defects (arrows) formed.

When a device or system fails many tests, and those failures stem from a specific type of IC defect, the device manufacturer and PCB assembler may choose from several quality-improvement strategies. Strategies could include failure analysis at the IC manufacturer that leads to improved production techniques and materials and to the reclassification of device moisture-sensitivity levels. PCB assemblers can shorten their allowed floor-life periods, change solder-reflow-oven temperature profiles, and ensure the proper storage of moisture-sensitive ICs.

If you experience failures of a specific IC or packaged device, monitor your own manufacturing processes and consult with the device manufacturer about possible moisture-sensitivity problems. By working together, you can determine how to avoid problems. T&MW

REFERENCE

1. "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices," IPC/JEDEC J-STD-020D, June 2007. www.jedec.org/download/search/JSTD020D.pdf.

Tom Adams *is a freelance writer and consultant who has published numerous articles in semiconductor and microelectronics trade magazines. teadams@earthlink.net*

Steven R. Martell *is the manager of technical support services at Sonoscan. He serves as chairman of the IPC's B-10a—Plastic Chip-Carrier-Cracking Task Group and has received several awards from IPC and JEDEC for his leadership of standardization efforts.*

Handheld multimeter logs data

Fluke's 287 digital multimeter (DMM) can store up to 10,000 readings and lets you download data through its optically isolated serial port that connects to a PC's USB port. It can record multiple logging sessions, eliminating the need to download data after each session. You can plot logged data on the 287's 1/4 VGA screen, or you can display measurements such as volts along with minimum, maximum, and average readings.

The meter features a 50,000-count backlit display that measures DC and true-RMS AC current and voltage, resistance, diode check, capacitance, frequency, duty cycle, and pulse width. The 287 has a 100-kHz AC bandwidth, and it can measure current up to 10 A (20 A for 30 s). As a capacitance meter, the 287 has a low-impedance input mode so it can dissipate the charge in a capacitor, thus providing a true reading.

Basic DC accuracy is 0.025% with true-RMS AC accuracy of 0.4%. Its 500.00-Ω resistance-measurement range lets you measure resistance with 10-mΩ resolution.

Price: $499.95. *Fluke, www.fluke.com.*

Waveform generators feature 27 functions

The 4084AWG and 4086AWG arbitrary/function generators can produce 27 standard and complex waveforms with sine-wave frequencies up to 20 MHz and 80 MHz, respectively. The instruments produce arbitrary waveforms at sample rates up to 200 Msamples/s. Both models are programmable through either a knob or keypad, letting you select frequency or period. You can also select signal amplitudes on V_{PP}, mV_{PP}, V_{RMS}, mV_{RMS}, or dBm.

The instruments come with software that lets you import measured signals from a Tektronix oscilloscope (Models TDS1000, TDS2000, TPS2000, or TDS3000).

Using the RS-232 port, you can download waveforms from the oscilloscopes or create your own waveforms to download. For automated applications, you can program the instruments using SCPI commands.

Prices: 4084AWG—$1295; 4086AWG—$1895. *B&K Precision, www.bkprecision.com.*

R&S FSU67 spectrum analyzer covers 20 Hz to 67 GHz in single sweep

The Rohde & Schwarz FSU67 spectrum analyzer covers the 20-Hz-to-67-GHz frequency range in one full-span sweep with a single coaxial input without the need for external harmonic mixers. The FSU67 also has an integrated instrument-controlled RF attenuator with a range of 0 to 75 dB in 5-dB steps that eliminates the external manually operated attenuator required when harmonic mixers are used. The instrument's reference

level range (–130 dBm to +30 dBm) is also higher than can typically be achieved with harmonic mixers.

In addition to being appropriate for research and development environments, the R&S FSU67 is suited for use on the production line. It provides IEEE 488 or Ethernet LAN connectivity and includes USB interfaces. The instrument is also certified as being compliant with LXI Class C. It can make 80 measurements/s in manual mode and 70 measurements/s over the IEEE 488 bus. The instrument will also control external signal generators via the IEEE 488 or TTL bus to act as tracking sources for making scalar transmission, loss, and reflection measurements.

Specifications for the R&S FSU67 include a noise floor of –158 dBm at 1 GHz and –130 dBm at 65 GHz, resolution bandwidth of 1 Hz to 50 MHz, display linearity of less than 0.1 dB, total measurement uncertainty of less than 0.3 dB, and frequency resolution of 0.01 Hz. Phase noise at 640 MHz ranges from –104 dBc at a 100-Hz offset to –160 dBc at a 10-MHz offset.

The R&S FSU67 can perform as a fully featured RF power meter with instantaneous display of measurement results when coupled with one of the company's R&S NRP Series power sensors. Sensor calibration factor is automatically applied along with the selected center frequency. In addition, channel and adjacent-channel power can be determined with the instrument's time-domain power-analysis capability and channel or RRC filters.

Rohde & Schwarz, www.rohde-schwarz.com.

Agilent debuts EXA economy signal analyzer

Agilent Technologies' EXA signal analyzer provides flexible, scalable signal analysis to budget-conscious engineers. At a lower performance point than Agilent's MXA signal analyzer, the EXA includes a set of standard one-button measurements for characterizing signal quality. It measures adjacent-channel power ratio (ACPR), channel power, occupied bandwidth, power complementary cumulative distribution function (CCDF), burst power, and spurious emissions. It also includes a spectrum-emissions mask function.

Optional measurement application software provides preconfigured test routines for GSM/EDGE, 802.16e Mobile WiMAX, W-CDMA, HSDPA/HSUPA, and phase-noise applications. Running the Agilent 89600 VSA software application in the EXA enables signal demodulation analysis and troubleshooting of more than 50 demodulation formats, including 2G, 3G, 3.5G, WiMAX, WLAN, and Private Mobile Radio.

The EXA returns a marker peak search result in less than 5 ms, local updates in less than 10 ms, and a remote sweep and transfer (via GPIB) in less than 12 ms. Measurement mode switching speeds are typically less than 75 ms.

The EXA signal analyzer supports multiple frequency ranges from 9 kHz to 3.6, 7.0, 13.6, and 26.5 GHz, an internal fully calibrated pre-amplifier option up to 3.6 GHz, and standard analysis bandwidths of 10 MHz. This fully scalable functionality is complemented by EXA's +13-dBm third-order intercept, –146-dBm/Hz displayed average noise level (without pre-amp), and 66-dB W-CDMA ACLR dynamic range, as well a 0.4-dB total absolute amplitude accuracy, which is made possible by the all-digital, 14-bit ADC IF section.

Base prices: from $16,900 for a 3.6-GHz model to $35,900 for a 26.5-GHz model. Option prices start at $1000. *Agilent Technologies, www.agilent.com.*

Intepro Systems debuts LXI power supply test system

Intepro Systems has announced its first LXI-based power supply test system, the I-9500LXI. The tester comes with a six-digit multimeter and four-channel digital oscilloscope, five test loads, an 850-VA AC

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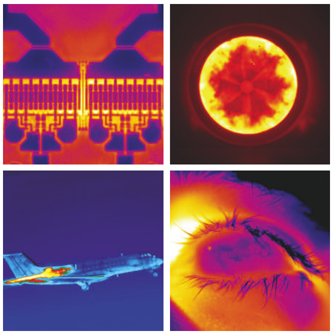

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power source, and Intepro's PowerStar 5 software. It supports legacy test instruments that communicate using RS-232C and IEEE 488.2 while providing a migration path to future LXI instruments.

The base system has a single 300-W load and four 75-W loads, an 18-input-by-4-output differential multiplexer, 16 digital inputs and 16 digital outputs, 48 relay drivers, and 10 5-A power relays. The architecture can also accommodate 850-VA AC, 1250-VA AC, or 1500-W DC power sources.

Intepro Systems, www.inteproate.com.

Digitizer card streams in four lanes

The ATS9462 PCI Express (PCIe) digitizer card from AlazarTech has no onboard memory because it doesn't need any. Using four PCIe lanes, the card can stream data to PC memory at a sustained rate of 720 Mbytes/s. That's fast enough to keep pace with the card's two 180-Msample/s analog input channels.

As with other four-lane PCIe cards, you can plug the ATS9462 into any available four, eight, or 16-lane PCIe slot. Sample rates range from 1 ksample/s to 180 Msamples/s. Digitizer inputs have 16-bit resolution and 65-MHz bandwidth. Input voltage range is ±200 mV to ±16 V. DC accuracy is ±2% of range for all input ranges. Input impedance is 1 MW but you can change that to 50 W for RF applications using a DIP switch on the card.

The ATS9462 uses two trigger engines, called X and Y. You can combine the two engines using logical OR, AND, or XOR operands, then specify the number of records to capture in an acquisition, the length of each record, and the amount of pretrigger data.

The card includes software that lets you operate the card, acquire data, and store data. Optional software-development kits are available for C/C++, Visual Basic, LabView, and Linux.

Price $4995. *AlazarTech, www.alazartech.com.*

OTDR enables testing at up to 250 km

EXFO offers the FTB-7600E optical time-domain reflectometer (OTDR) for ultra-long–haul network applications. With a dynamic range of 50 dB, the OTDR can characterize links up to 250 km and offers a linearity of ±0.03 dB/dB.

The FTB-7600E is housed inside the FTB-200 Compact Platform for technicians requiring a multi-technology test platform for large-scale

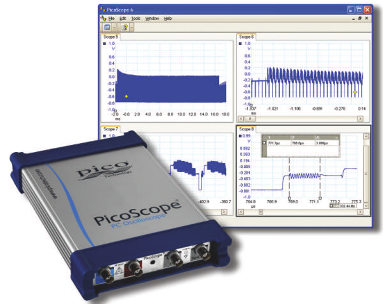
network deployments. It is also available for the FTB-400 universal test platform, which is designed for network engineers who need advanced network diagnostics.

The OTDR module comes in single and dual-wavelength configurations and delivers up to 256,000 sampling points to achieve high trace resolution. A single push of a button generates detailed results, including a complete event table, within 5 s.

EXFO Electro-Optical Engineering, www.exfo.com.

PC-based scopes sample at 1 Gsample/s

Pico Technology claims that its PicoScope 5000 series of USB PC oscilloscopes delivers the bandwidth, sampling, and memory depth of expensive conventional benchtop oscilloscopes at prices starting at just over $2400. Both the PicoScope 5203 and PicoScope



5204 provide two channels plus an external trigger, a probe-tip bandwidth of 250 MHz, 8-bit resolution, and a real-time sampling rate of 1 Gsample/s (single channel). For repetitive signals, an equivalent time-sampling mode increases sampling to 20 Gsamples/s. The 5203 has a record length of 32 Msamples; the 5204 has a record length of 128 Msamples. The oscilloscopes come with PicoScope 6 oscilloscope software, which lets you use the card as an oscilloscope, spectrum analyzer, or meter.

Pico Technology, www.picotech.com.

Prism Sound upgrades audio analyzer software

In Version 1.21 of its dScope Series III audio analyzer software, Prism Sound has added tools for acoustic measurements, PC audio, and 192-kHz sampling on digital audio interfaces. Key features of Version 1.21 include generation and analysis using Windows sound devices, support for acoustic measurements of transducers and rooms, fast measurements (including frequency response) using a swept-sine (Farina) method or bin-centered noise with impulse response and fast Fourier transforms (FFT), and quasi-anechoic measurement using an adjustable time window to eliminate acoustic reflections.

The software also performs microphone sensitivity measurements and frequency response calibration, as well as time domain averaging to reduce the effects of random noise on measurements. Analog I/O can now sample at 48 kHz, 96 kHz, and 192 kHz to increase low-frequency resolution of FFT analysis. A script debugger allows breakpoints, single stepping, and examination and setting of variables.

Prism Sound, www.prismsound.com.

Yokogawa expands optical-component test system

Three new modules are available for the AQ2200 Multiple Application Test System (MATS) from Yokogawa, providing expanded functional performance, lower testing cost, and improved efficiency. The AQ2200-215 optical sensor module measures +30 dBm at 10,000 samples/s and can be used for power measurement and margin testing of WDM transmission equipment. It is also designed for output power and gain testing of optical fiber amplifiers. The AQ2200-412 is a 1x16 optical switch module for testing multiple devices.

The third module, the AQ2200-641 XFP test interface module, provides full signal control and access to a 10-Gbit small form factor pluggable (XFP) transceiver with independent data in and out, bar data in and out, and reference clock in. All XFP transceiver functions are accessible, allowing you to read, write, and control the XFP itself.

Yokogawa, www.yokogawa.com.

Spirent tester validates triple-play service

Enhancements to Spirent's Tech-X Plus field tester enable technicians to validate triple-play services at xDSL access points, as well as over the homeowner's wireless network. Tech-X Plus increases the efficiency of triple-play service deployment with a modem that supports ADSL to VDSL2 and 802.11b/g wireless for testing and communicating with back-office systems. It verifies that VDSL/VDSL2 rates are sufficient to support bandwidth-intensive services, such as IP video, and subsequently tests the service anywhere along the local loop and within the customer's home to enable rapid fault location.

Spirent Communications, www.spirent.com.

Strain-gage interface handles military applications

Electro Standards Laboratories' CellMite ProD Model 4333 is a data-acquisition and strain-gage interface board for embedded military and industrial applications that require high-speed analog and digital data acquisition. The CellMite ProD provides dual 24-bit independent strain-gage channels that sample at 15 ksamples/s. Alternatively, the board can be configured with four channels sampling at 5 ksamples/s.

The CellMite ProD also furnishes 12 additional 12-bit analog input channels with a throughput of 1 Msample/s, as well as 64 bits of digital input sampled at 20 Msamples/s. Four 16-bit analog output channels offer user-selectable scaling and offset with a range of ±10 V. For applications requiring onboard data storage, the CellMite ProD supplies 1 Mword of memory, along with an SD card slot for additional data storage.

Electro Standards Laboratories, www.electrostandards.com.

Finisar delivers 10GbE protocol analyzer for FCoE

Finisar has unveiled the Xgig 10GbE analyzer, which supports the ANSI Fibre Channel over Ethernet (FCoE) initiative. The Xgig platform can be used for testing protocols such as Fibre Channel, SAS/SATA, Ethernet, and iSCSI.

The FCoE option consists of a blade that plugs into the Xgig platform, expanding the analyzer's capability beyond the current 8-Gbps Fibre Channel and 6-Gbps SAT/SATA rates. In addition to supporting FCoE, the 10GbE analyzer can monitor up to 32 ports so developers can analyze all traffic passing over a link. Xgig supports multiprotocol synchronous capture to allow the correlation of packets as they cross protocol domains.

Finisar, www.finisar.com.

MACHINE-VISION & INSPECTION

TEST REPORT

Throughput needs drive vision-system camera choices

By Steve Scheiber, Contributing Technical Editor

User expectations for cameras in electronics manufacturing have changed, and not always in obvious ways. I asked Mark Butler, product manager at Dalsa Digital Imaging, for his take on the implications.

Q: What camera features do electronics manufacturers look for today?

A: A lot depends on the application—pick-and-place has different needs from AOI, x-ray, or layer-upon-layer bare-board inspection. Some companies choose analog cameras for pick-and-place, for example, often using as many as 20 to ensure proper component position. Cameras mounted inside production equipment can provide a troubleshooting tool for the equipment itself.

Q: What is the most significant factor driving manufacturers' choice of camera?

A: Everyone wants high-quality images and wants cameras to be small and easy to use. But our customers' number one priority is throughput—how fast they can inspect their boards.

A few years ago, we introduced a 2-Mpixel camera that took 30 fps and a 4-Mpixel camera at 15 fps. With the larger number of pixels, the camera can see more of the board in each image and can cover the board with fewer images. As parts and other board features continue to shrink, however, you need higher resolution to maintain the same field of view. That's why we introduced the 4M60 camera that produces 4-Mpixel images at a full 60 fps.

Q: Why has higher resolution become such an imperative?

A: No matter how small features become, inspecting them requires the same number of pixels. If you need 5 pixels to detect a bad lead, as the leads get smaller, you still need 5 pixels, but they cover a smaller area. Either you have to increase the camera resolution or cope with a larger number of images to cover the entire board surface.

Q: What are the consequences of needing higher resolution?

A: Most high-speed camera imaging chips use "rolling shutter" CMOS technology, which acquires the image in a series of rows—up to the imager's maximum. The technique exhibits time-domain effects. If either the object under inspection or the camera is moving, each row is acquired at a different moment in time and therefore a different point in space. Straight lines can look slanted. The image is less precise than it could be.

We designed a special CMOS chip with a global shutter that captures the entire frame at once to avoid that effect. It can also integrate one image while reading out another, increasing the camera's effective frame rate.

Q: Do you lose throughput while repositioning the camera?

A: While the camera is in one place, the system takes a complete set of images, changing color, lighting, incidence angle, and so on. You perform image analysis while the camera moves to the next location, in say 200 ms. That way you can maximize your efficiency and throughput. In other cases, the board moves rather than the camera itself. □

Mark Butler
Product Manager
Dalsa Digital Imaging
Courtesy of Dalsa Digital Imaging

INSIDE THIS REPORT

EDITOR'S NOTE

Gathering the quality evidence

Steve Scheiber, Technical Editor

Creating a workable, economical test and inspection strategy often seems like a bit of a black art. We apply all of our experience, yet we wonder if we are looking for the defects that the boards actually contain. Gathering good defect data is expensive and time-consuming, so we often don't have a lot to work with.

Eight years ago, when Stig Oresjo, then with Agilent Technologies, analyzed his original data on more than a billion solder-joint defects from 15 companies—including both OEMs and contract manufacturers—he shed some light on the situation. His results showed that the vast majority of defects consisted of shorts (22%), opens (46%), and insufficient solder (17%). More significantly, he discovered that the average number of defects per million opportunities (DPMO) vastly exceeded manufacturers' goals.

Oresjo has now released a new study that shows progress achieving better quality, despite increased product complexity. Test strategies have changed somewhat, and because this time he included companies from Asia, they proved less consistent. The article on p. 68 in this issue examines some of his results.

Much analysis remains to be done—3.7 billion solder joints do not surrender their secrets easily. It will be interesting to see what new insights they will reveal—and how the next study eight years from now will compare. □

Contact Steve Scheiber at sscheiber@aol.com.

HIGHLIGHTS

EyeSpector version 1.5 debuts

EyeSpector, a cooperative enterprise of Vision Components and SAC, has introduced version 1.5 of its drag-and-drop machine-vision sensor family for generic measurement and gauging tasks. The new EyeSpector software adds 20 graphically programmable image-processing functions as well as support for 2-D/3-D calibration and communication with robots. Enhanced communication functions allow for data transfer among several smart cameras and hosts, expanding applicability to multicamera and 3-D applications.

The EyeSpector works with the VC4xxx real-time and network-ready Smart Camera series—including all color, line scan, and megapixel models up to 240 fps.

With EyeSpector, users also can process rotated images and transmit classification results with subpixel accuracy. EyeSpector provides for brightness compensation using histogram algorithms, pattern matching, color measurements (based on RGB or HSI color models), and position compensation (horizontal, vertical, and rotary angles). Advanced users can take advantage of the software's built-in VB 6.0-compatible Basic interpreter. Base price: $2000. www.eyespector.com.

Flir to acquire Cedip Infrared

Flir Systems has announced that it has agreed to acquire a controlling interest in Cedip Infrared Systems, a provider of infrared cameras and stabilized gimbaled systems based in Croissy-Beaubourg, France. Founded in 1989, Cedip manufactures cooled mid- and long-wave infrared cameras for the science and security markets as well as stabilized gimbals for air-

Tips for triggering FireWire cameras

Implementing inspection requires you to find the best way to trigger a camera so your images capture the right information. National Instruments recently published two tutorials on its Web site that address this challenge for FireWire cameras.

Although aimed primarily at users of NI's LabView and Vision Builder, the tutorials provide a great deal of information that applies to any image-acquisition situation. They describe general triggering concepts, including "free run mode," which is the default operation of most cameras, along with both hardware and software triggering. In addition, the tutorials provide a summary of the FireWire (IEEE 1394) bus and its isosynchronous and asynchronous operation. Like their analog cousins, FireWire-compliant cameras require an extra signal line to carry the trigger, because the 1394 bus cannot send a trigger directly.

A description of the six conventional triggering modes defined by the standard includes the caveat that not all cameras implement all six modes. Therefore, you must choose a triggering scheme based on the capabilities of the camera for the target application. The tutorials also emphasize the need to account for latency, which defines the time lag between the trigger signal and the actual image capture. A trigger configuration example is accompanied by diagrams that make the explanation more tangible.

The tutorials are basically identical except for the software that they address: "Triggering a FireWire Camera Using LabView on a Compact Vision System" and "Triggering a FireWire Camera Using Vision Builder AI on a Compact Vision System." www.ni.com.

borne commercial and government applications. Flir manufactures thermal-imaging and stabilized camera systems for thermography and imaging applications.

Controlling shareholders of Cedip have agreed to sell shares representing 67.8% of the share capital of Cedip for approximately $57.1 million. The transaction is subject to various closing conditions, including the authorization of the French Minister of Finance and Economy.

Upon completion of the transaction, Cedip's infrared camera operations will be integrated into Flir's Thermography Division. Its Polytech subsidiary (airborne imagery and gimbals) will be integrated into Flir's Government Systems Division.

"We are pleased to announce this transaction," commented Earl Lewis, chairman, president, and CEO of Flir. "The Cedip team has an outstanding reputation for designing and manufacturing high-performance cameras and will provide Flir with complementary products and capabilities to help drive growth in key market segments worldwide." www.flir.com.

Adimec cameras inspect shuttle damage

Adimec reports that the recent Space Shuttle Endeavour mission relied on the company's cameras to determine the threat of damage from a gouge in the shuttle's protective tiles. The damage was caused by debris that broke away from the spacecraft and struck the tiles soon after launch.

Adimec says that to analyze damage and determine if the shuttle would be cleared for landing, the shuttle astronauts took over 1500 high-resolution images with the Adimec camera system. "We are pleased that images from our cameras were able to play an important role in helping the shuttle and crew fly home safely," said Jay Rice, VP of sales and marketing for Adimec in North America.

CALENDAR

- **Vision 2007**
  November 6–8
  Stuttgart, Germany
  Produced by Messe Stuttgart
  www.messe-stuttgart.de

- **AIA Business Conference**
  January 29–31
  Orlando, FL
  Automated Imaging Association
  www.machinevisiononline.org

Adimec supplied multiple high-performance cameras to NASA; the cameras were coupled to Pleora's iPORT IP engine, which enabled them to stream high-resolution images to a laptop inside the shuttle over a standard Ethernet link. The imaging system was mounted at the end of the space shuttle's 50-foot robotic arm and controlled by the crew. www.adimec.com.

AIA names new managing director

The Automated Imaging Association (AIA), an international trade group for the machine-vision and imaging industry, has announced the promotion of Dana Whalls to managing director. Whalls has more than 18 years of experience in marketing, business development, and finance. She has served as marketing and public relations manager for the AIA since 2004.

"In the three years Dana has been with AIA, she has played a pivotal role in our growth to more than 280 member companies in 26 nations. She has helped us expand our research in Europe and Asia, which is critical to our mission to promote machine vision on a global basis," said Jeff Burnstein, executive VP of the Automation Technologies Council, the umbrella organization governing the AIA and its sister associations, the Robotic Industries Association and the Motion Control Association. www.machinevisiononline.org.

Solder-joint study shows defect levels remain above targets

By Steve Scheiber, Contributing Technical Editor

In 1999, Stig Oresjo, then of Agilent Technologies, conducted a major study of solder-joint defects on printed-circuit boards (PCBs). The study, which at the time provided the most definitive data on the subject, involved 15 companies and more than 1 billion solder joints. Oresjo concluded that although companies claimed defect levels in the range of 75 to 150 defects per million opportunities (DPMO), the reality was 5 to 10 times that high.

Now retired, Oresjo has returned to the well one more time to see if the situation has changed. In a new analysis, he tabulated 3.7 billion joints—almost four times as many as in the previous study—from 1100 different board types at 14 companies, again including both OEMs and contract manufacturers.

Whereas the first study included companies only from the US and Western Europe, this time Oresjo studied two companies in the US, four in Europe, and eight in Asia. His results suggest that although board quality has improved in the past eight years despite increased complexity, defect levels still do not live up to manufacturers' claims.

Oresjo described the new study this way: "To reduce the number of random variables, we restricted the sample to companies using [Agilent's] 5DX x-ray inspection systems, as well as datalogging software that we could read easily, thereby facilitating the analysis. To encourage participation, I agreed not to reveal company names. Boards under test ranged from medium to high complexity.

"We excluded low-complexity boards because we wanted boards that routinely underwent x-ray inspection, often not practical at low complexities. Production volumes covered the entire range, as did product mix.

"We considered every solder joint that was inspected to be a defect opportunity, ignoring any joint that bypassed that step. Every defect that the 5DX caught and that was later verified as a defect counted toward the total. I did exclude data from any board that went through the inspection process several times in quick succession and any board that was inspected during program development rather than production, and limited each company to the most recent 500,000,000 joints in the data they provided. I developed software in Visual Basic to read the data and convert it to a Microsoft Access database.

"If the inspection step flagged a defect, but it was never verified as real and repaired, we removed the entire board from the analysis. Only about 1% of the boards fell into a category where the data were not used. We didn't look at false calls, only verified defects in relation to the total number of defect opportunities.

"Even achieving defect levels similar to those in the earlier study would have been an accomplishment. Today's boards are much more complex. Also, manufacturers are much more cost-conscious, and when belts tighten, test tends to take a big hit. But the situation has improved more than that.

"In the first study, we found an aggregate average of 1083 DPMO. This time, defects totaled 572 DPMO. We broke the data down further into 327 DPMO for actual defects that underwent repair and 245 DPMO for process indicators.

"We differentiated between the two based on the repair operator's judgment on whether to fix a problem before sending the board on to the next step. Process indicators might not require immediate action, but if there are enough of them, they should trigger adjustments to the process.

"Insufficient solder, for example, can be a process indicator or a defect. It may not cause a board to fail, but it can still compromise the board's reliability in the field. Expansion and contraction caused by powering up and powering down the board can make the joint fail, as can excessive handling. Reducing or eliminating this problem might mean cleaning the solder mask. Another reason for tracking process indicators is that, in our experience, manufacturers who experience a lot of them also tend to have a higher rate of repairable defects."

SOLDER-DEFECT STUDY, 1999 VS. 2007

	1999	2007
Companies	15	14
US companies	9	2
European companies	6	4
Asian companies	0	8
Board types	566	1100
Solder joints	1 billion	3.7 billion
DPMO—total	1083	572
DPMO—defects	Not determined	327
DPMO—process issues	Not determined	245

Changes in processes

Although Oresjo expressed no doubt that board quality has improved in recent years, he pointed out that the processes have changed somewhat, making the data more difficult to compare directly with the earlier study.

"More companies are using visual inspection than did in 1999," he commented. "In Asia, that inspection might be more manual than in the US and Western Europe where AOI [automated optical inspection] is more common, but either way, some defects that would have shown up before would not have survived as far as the x-ray system this time. Visual inspection catches the lowest-hanging fruit, so to speak."

When asked what surprising results showed up in the data, Oresjo responded, "We found defects on all kinds of components and solder joints—gull wings, BGAs [ball-grid arrays], connectors, resistors, and so on. Some of them were naturally hidden from optical inspection, but others should have been visible to optical inspection. We would have expected those to be caught at the earlier step."

Despite the data generated by the study, manufacturers commonly still quote much lower defect rates. Contract manufacturers often stick with the 75 DPMO that they have been touting for years. When asked about the discrepancy, Oresjo explained, "The lower numbers can be supported if you realize that they are calculated under best-case conditions. Companies use the most stable boards in production, the best-controlled processes, the best production days, and so on. If all contract manufacturers signed up to the higher numbers, they would show up more frequently. But companies look at the others' claims and realize that they have to quote numbers obtained under similar conditions in order to compete. You can probably find the more realistic numbers internally within OEMs, because there they are used to guide engineers and managers to product and process improvements."

How do companies react when they see the study results? Oresjo put it this way: "Not as many people have seen this data as saw the previous study. But the response is generally the same—a room full of smiles and nodding heads. Industry people have a very good idea about the real-world situation. They use the data during manufacturing and during development to improve both processes and products. Awareness of real defect levels is very important. If defects escape to customers, they cause warranty and other field failures, incurring both high costs for correction and a loss of goodwill." □

Lighting and software improve AOI results

By Steve Scheiber, Contributing Technical Editor

The ability of automated optical inspection (AOI) techniques to find board faults depends as much on issues such as lighting and contrast as it does on the capabilities of the inspection systems themselves. In addition, using the same architecture for both benchtop development systems and for systems in production simplifies the implementation of an inspection strategy. Josh Petras, product manager at YESTech, has devoted a lot of his energy to these issues, incorporating the principles into the company's latest line of AOI systems.

"Lighting has to be flexible," said Petras. "A flexible lighting system enables better defect detection and faster cycle times. Techniques such as 'fusion lighting,' which detects specific features by incorporating multiple colored lights from different angles and color filters, are invaluable when dealing with ever-changing PCB complexities."

Petras compared this type of analysis to the information on a topographic map. "A topographic map allows you to visually extract 3-D information from a 2-D image. The fusion lighting concept works the same way. Since structured lights are projected from different angles onto various surfaces of the board, the reflected light is also colored. Low-angle surfaces reflect mostly red light, while medium angles and steep angles reflect primarily green and blue, respectively. The software color filters allow the inspection algorithms to isolate specific color spectra that relate directly to their slope and orientation in three dimensions."

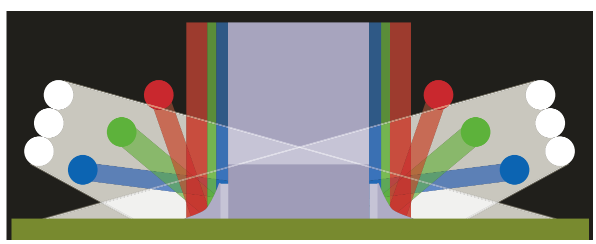
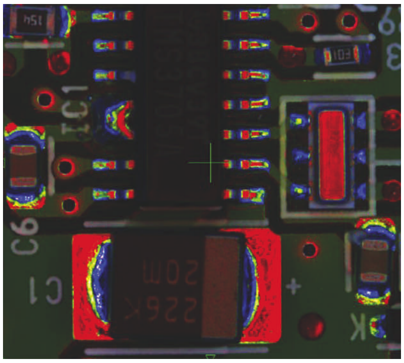


Fig. 1 Incident lighting of several colors at different angles produces an aggregate image. Courtesy of YESTech.

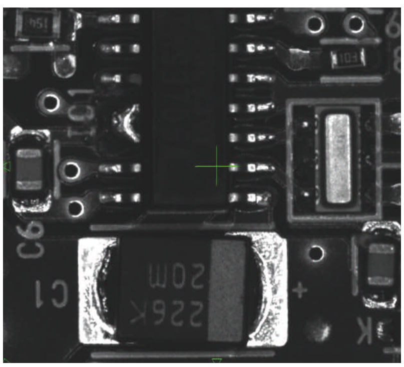
Figure 1 illustrates a fusion lighting configuration that includes both incident white light and red, green, and blue lights that come in from different angles. The colored lights produce the aggregate image in **Figure 2a.** Figure 2b shows the result of applying a red filter, rendered as a gray-scale image. Figure 2c shows the same board area through a green filter, and Figure 2d through a blue filter. Examining the image as though illuminated only by red light reveals joints with insufficient solder. The leads themselves show up better in blue light. The white light version of the image allows the identification of part markings and the examination of part orientation.

"We are not necessarily looking for a high frame rate with this technique," remarked Petras. "We would rather combine the information into fewer images taken at higher-resolution and then perform the analysis in software.

"We are not the first company to employ lighting at different angles to enhance image contrast, but we believe our unique software approach enables better results while simplifying the overall user experience. Other companies rely on multicolored light structure for all of their inspection points. We include white-light sources



a)



b)

c)

d)

Fig. 2 Filtering the aggregate image in (a) with a red filter produces (b). A green filter reveals the details in (c), while a blue filter shows image (d). Courtesy of YESTech.

independent of the RGB composite, which is more effective for the white-light part of the analysis. We wanted to take advantage of the power of today's off-the-shelf PCs by putting more of the throughput burden on the software."

To verify that the new configuration improves results, YESTech compared inspections performed with the multicolor lighting scheme to similar inspections from their previous AOI systems that relied primarily on white and red light. Although those systems could use color filters, they didn't take advantage of the feature very often. "The new arrangement produces images with more information for our inspection algorithms, and ultimately a more consistent and robust test," said Petras. "Based on internal benchmarks and customer feedback, detection has gone up and false calls have gone down substantially, especially on very dense boards."

Petras also advocates using benchtop and production systems that share an architecture. "The standardization allows an engineer to capture an image on the in-line system, then return to a desktop PC to create the inspection program. The benchtop version of the system can also work well in a repair station or quality cell. The overriding consideration is yield management.

"A common architecture makes managing the operation, as well as collecting, archiving, and analyzing the resulting data much easier. You can build a database, create historical reports, or implement Web-based statistical control. Critical information can be extracted at various points in the process."

He added, "The common architecture helps ensure data consistency and improves the quality of the subsequent analysis." □

PRODUCTS

Camera Link interface for recording system

A mezzanine board for Conduant's StreamStor Amazon digital data recorders provides connectivity for one or two Camera Link cameras at data rates of up to 500 Mbytes/s. Combined with the direct-to-disk capability of the StreamStor Amazon recording system, the CL-500 Camera Link interface board enables the high-speed and long-duration recording required when shooting high-resolution or high-frame-rate digital video.

The CL-500 accommodates nearly any Camera Link full, medium, or base configuration. It employs fast Channel Link components and programmable logic to deliver a flexible platform for digital video recording. *Conduant, www.conduant.com.*

PCIe Camera Link frame grabbers

The MVS-8600e family of frame grabbers from Cognex connect Camera Link cameras through the PCI Express (PCIe) interface. The frame grabbers are available in single-channel and dual-channel models and include machine-vision software tools that locate objects or patterns, measure their geometric properties, detect defects, and read characters and codes. *Cognex, www.cognex.com.*

Machine-vision illuminator

Dolan-Jenner has introduced an improved version of its Fiber-Lite DC-950H fiber-optic machine-vision illuminator. The 150-W quartz halogen regulated illuminator now produces a higher output with greater reliability, according to the company. It features DC-regulated output, fast lamp response, and a 0–5-VDC remote intensity-control interface with linear voltage adjustment. Available options include color filtering, manual iris, and an analog or digital remote interface. *Dolan-Jenner Industries, www.dolan-jenner.com.*

5-Mpixel GigE camera

Prosilica's GC2450 camera runs at 15 fps with a 2456x2048 resolution over a Gigabit Ethernet (GigE) Vision interface. The 33x46x43-mm camera uses Sony's 5-Mpixel ICX-625 progressive-scan CCD sensor with a global electronic shutter for capturing high-speed motion events. Features include programmable exposure controls, area-of-interest readout, advanced binning modes, 12-bit readout, asynchronous external trigger and sync I/O, and an RS-232 peripheral port. *Prosilica, www.prosilica.com.*

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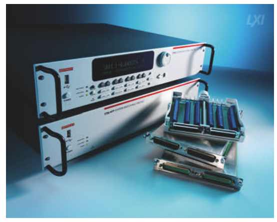

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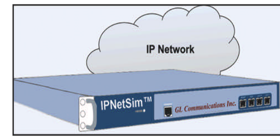

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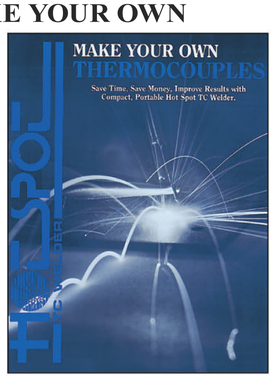

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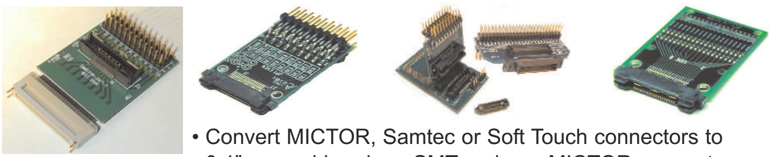

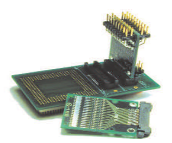

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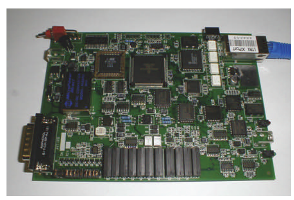

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HELMUT BERG
President
JDSU, Communications Test & Measurement
Germantown, MD

Helmut Berg brings more than two decades of technical and executive management experience to JDSU. He joined the company in 2005 when it acquired Acterna, where he had been division president leading the development of some of its most successful lines of test instruments and systems. Earlier in his career, Berg held executive positions with Honeywell and Tektronix. He holds BS and MS degrees in computer science from the Universitaet des Saarlandes in Germany, and he also earned a PhD in computer science from the University of Minnesota and completed the General Management Program at the Wharton School.

Contributing editor Larry Maloney conducted a phone interview with Helmut Berg on trends in the communications test field.

How broadband hunger fuels test

Q: How far has the communications industry rebounded from its early-decade slump?

A: It's been a gradual recovery, but lately it has accelerated. JDSU has benefited from the build-out of new broadband networks and adoption of bandwidth-intensive services, such as VoIP and IPTV. Growth in on-demand content, such as YouTube and iTunes, also drives new network challenges and increases the need for test solutions.

With these trends, JDSU is in a unique situation, since our test portfolio addresses the entire network and service deployment life cycle. This ranges from development and production in the network-equipment manufacturer arena to deployment in the field and then ongoing service assurance and network monitoring. We provide test products to the cable industry and the telecom industry, and the competition between those sectors to lock in customers with a compelling package of services has helped drive double-digit growth in our communications test business.

Q: What portion of JDSU's total business can be attributed to test and measurement?

A: Test and measurement is the largest segment and is tracking at about $600 million in annualized revenue. In the most recently reported quarter (ending March), the T&M business grew by 28%. We also see strong performance in other JDSU units. For example, JDSU is the leader in the ROADM [reconfigurable optical add-drop multiplexer] market and enjoyed record shipments in the quarter ending March 31. Our Advanced Optical Technology group and our laser businesses also are growing at double-digit rates.

Q: How has the test and measurement business evolved at JDSU?

A: Our heritage was field-service test, which includes test instruments carried by technicians, and that remains our largest segment. From that core, we have expanded to other areas, such as the network equipment manufacturer market, where we provide high-end instruments for system design, verification, and production. JDSU has also established the leading market position in 40G network test. Finally, we offer test systems that combine software and instrumentation into service-assurance solutions, as well as wireless service-assurance systems and software.

Q: What impact have recent acquisitions had on the company?

A: The acquisition of Acterna two years ago made JDSU the world's largest provider of test solutions to telecom and cable network operators. We followed that with three more important acquisitions: The acquisition of Test-Um expands our portfolio in home wiring and home testing. The Casabyte acquisition allows us to provide service-assurance solutions for the wireless market, and the acquisition in May of Innocor adds more broadband test solutions for network equipment manufacturers.

Q: What is the potential for home-networking test?

A: The intense competition between telecom, cable, and satellite service companies means that test service providers must take greater responsibility for the wiring inside homes and enterprises. There's great opportunity in this market.

Q: Which of your markets is now growing the fastest?

A: It's clearly broadband network deployment and services, which again points to the importance of the Innocor acquisition. We believe our enhanced capabilities put us in an even better position to help equipment manufacturers keep pace with next-generation technologies. T&MW

Helmut Berg provides additional comments on his company's products, services, and customer outreach programs in the online version of this interview: www.tmworld.com/2007_10.